Thank-You State of the Journal Editorial by the Outgoing Editor-in-Chief

Paolo Montuschi

THANK you! At the end of my 4th year of service as the Editor in Chief (EiC) of the IEEE Transactions on Computers (TC), these are the only two words that I can say, to express my sincere gratitude to all of you for your contribution to the success of the flagship Transactions of the Computer Society: Readers, Authors, Reviewers, Editors, Guest Editors, Topical Editors, Associate Editor in Chief, and IEEE & Computer Society Staff. Today the journal publishes an average of 12 high quality papers per issue and has further increased its impact factor from 2.916 in 2017 to 3.052 in 2018. This is the first time in its 67 years of life that TC that its impact factor goes above the value of 3. The capability to attract high quality papers involves a large number of factors, including the tradition of the journal and the reputation of its Editorial Board. As of November 1st (date of preparation of this editorial), the TC Editorial Board is composed of 72 members; it consists of 54 percent IEEE Fellows and 31 percent IEEE Senior Members; moreover it includes several top researchers who have received prestigious awards and recognitions. I am honored and proud to have had the opportunity to have worked with such an outstanding Editorial Board.

During the past 4 years, TC has gone through several changes and innovation has been one of our leitmotiv. Information has been provided through one or two editorials per year, as well as the TC web pages at https://www.computer.org/csdl/journal/tc and my personal page as EiC at http://staff.polito.it/paolo.montuschi/news-from-EIC-TC.html. Let me briefly summarize the three most important milestones that we have reached together. More details can be found in the editorials and directly in the issues of our journal.

1. Since January 2015, the featured paper of the month has a short presentation clip in English, prepared by the Authors and supervised by Professor Lan-Da Van of the National Chiao Tung University - Taiwan. Starting May 2015, TC has also a short video abstract in Chinese, posted on Youtube and Youku (and since a few months in 2018, also on the Tencent Video website). Professor Weiqiang Liu of the NUAA - PRC (chair of the multimedia team at TC) and Professor Yinhe Han of the Institute of Computing Technology (Chinese Academy of Sciences - PRC), have been in charge of the preparation of these videos. The production of a video clip presentation in Spanish was started in July 2016 by Professor Tomás F. Pena of the University of Santiago de Compostela - Spain.

2. In July 2016 editorial it was announced a speedup in the average turnaround time, inclusive for the largest majority of first time submissions receiving a first review decision in less than 100 days and more than 97 percent of all submissions (either in first or in revised form) in less than 120 days. Furthermore, the reduction of the backlog has shortened the accept-to-publication time; all accepted papers, as per IEEE Computer Society policies, after the upload by the authors of the final version, receive a DOI and become available for download and citation “as early access” manuscripts. As of today’s state of the queue (November 1st 2018), an accepted paper whose final files are uploaded today will be likely assigned to an issue between June and July 2019.

3. Starting January 2018 TC has redesigned the organization of its Editorial Board, by introducing the new role of Topical Editor (TE), whose task is to supervise contributions within a thematic area of interest of TC. Let me take this opportunity to thank the Colleagues who have served in 2018 as TEs, i.e., Professors Javier Bruguera, Ronald DeMara, Lieven Eeckout, Jean-Michel Muller and Patrick Schaumont. As expected, this new organizational model has been introduced to further improve the turnaround time (through a closer interaction between the TE and the AE) and simultaneously help the Editor-in-Chief in the day-by-day handling of the paper submission process. Nothing has changed from the viewpoint of the Authors, and the final decisions remain, as per IEEE and CS policies and procedures, the responsibility of the Editor-in-Chief.

In the past 4 years, more than 4800 decisions (accept, reject, major, minor, revise and resubmit as new, administrative reject) have been committed, i.e., an average of about 3.3 decisions per day (holidays and weekends included!). The largest majority of accepted papers (overall 700+) has gone through the major/minor/accept phases, in some cases even passing through a revise and resubmit as new.

The journal is in a very healthy state and it is my pleasure and honor to pass the token to Professor Ahmed Louri of George Washington University as the incoming Editor in Chief of TC. At the time when he was with the University of
Arizona, Ahmed and I worked together at the beginning of my service as he was an Associate Editor of TC. He is a highly reputed and visible researcher with interests and contributions in several fields, including not limited to: computer architectures, parallel and distributed computing, interconnection networks, fault-tolerant multiprocessors, network on chips, embedded and system on chips systems. Under his leadership, vision, wisdom and hard work, I am sure that TC will further grow and consolidate its leadership position.

In conclusion, while wishing all the best to Ahmed, let me renew my gratitude to all of you for your continued support and collaboration. Let me also take this opportunity for a special mention to two Colleagues who have been working very closely to me in my four years service: Ms. Natalie Cicero, the TC Assistant, and Dr. Javier Bruguera, TC’s Associate Editor in Chief.

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Ahmed Louri received the PhD degree in computer engineering from the University of Southern California, Los Angeles, in 1992. He is the David and Marilyn Karapet on Endowed chair professor of electrical and computer engineering in the George Washington University which he joined in August 2015. He is also the director of the High Performance Computing Architectures and Technologies (HPCAT) Laboratory. From 1988 to 2015, he was a professor of electrical and computer engineering at the University of Arizona, and during that time, he served six years (2000 to 2006) as the chair of the Computer Engineering Program. Throughout his career, he has held invited visiting scientist positions at various institutions, including the University of Electro-Communications (Chofu, Japan), the Communications Research Laboratory (Tokyo, Japan), the Laboratoire d’Informatique du Parallelism (Lyon, France), the University of Tsukuba (Tsukuba, Japan), the Universite de Paul Sabatier (Toulouse, France), and the Centre Nationale de Recherche Scientifique (Toulouse, France). From 2010 to 2013, he served as a program director in the National Science Foundation’s Directorate for Computer and Information Science and Engineering (CISE). He directed the core computer architecture program and was on the management team of several cross-cutting programs, including: Cyber-Physical Systems (CPS); Expeditions in Computing (EIC); Computing Research Infrastructure (CRI); Secure and Trustworthy Cyberspace (SaTC); Failure-Resistant Systems (FRS), Science Engineering and Education for Sustainability (SEES); and Cyber-Discovery Initiative (CDI), among others. He conducts research in the broad area of computer architecture and parallel computing with particular emphasis on interconnection networks, optical interconnects for parallel computing systems, reconfigurable computing systems, scalable & power-efficient architectures, Network on Chips (NoCs) for multi-core & many-core architectures, fault-tolerant & self-healing NoCs, emerging interconnect technologies (photonic, wireless, RF, hybrid) for multi-core architectures & Chip Multiprocessors (CMPs), embedded systems, and machine-learning enabled computing & networking. He has published more than 160 refereed journal articles and peer-reviewed conference papers in these areas, and holds several US and international patents. His research has been sponsored by the NSF, the Department of Energy (DOE), the Air Force Office of Scientific Research (AFOSR), and a number of industrial organizations including Intel, IBM, Cisco, Sun Microsystems (now Oracle), Raytheon, Physical Optics Corporation, and US West Technologies. He is a fellow of the Institute of the IEEE, a member of the IEEE Society Technical Committee on Computer Architecture, a member of the IEEE Technical Committee on Parallel Processing, and a member of the IEEE Computer Society Technical Committee on Microprocessors and Microcomputers. He is the recipient of the National Science Foundation Research Initiation Award (now called the NSF CAREER Award), the Best Article Award from the IEEE Micro, the Advanced Telecommunications Organization of Japan (ATOC), the Centre Nationale de Recherche Scientifique (CNRS, France) Fellowship, and the Japan Society for the Promotion of Science (JSPS) Fellowship, as well as several teaching awards. His early work explored Optics’ unique properties to advance computing and communications. He was instrumental in bringing optical interconnects into main stream research in computing and interconnection networks, and bridging the gap between computer architecture and optics research communities. He has served as a general chair for the 13th Annual Symposium of the High Performance Computer Architecture (HPCA-13, Phoenix Arizona, 2007); the general co-chair of the Second Workshop on Optics in Communications and Computer Sciences (WOCCS-99, Toulouse France, 1999); the general chair for the Workshop on Optics in High-Performance Computing Systems (Lyon France 1996). He was the founding member of the NSF Workshop on Emerging Technologies for Interconnects (WETI, Washington D.C. 2012), and the NSF Workshop on Cross-Layer Power Optimization and Management (CPROM, Los Angeles California, 2012). He is the general chair of the 25th Annual High Performance Computer Architecture, HPCA 2019 to be held in Washington DC, Feb. 2019. Dr. Louri currently serves as Associate Editor for the IEEE Transactions on Emerging Technologies for Computing (2015 – present), and the IEEE Transactions on Sustainable Computing (2016 – present). Since Jan. 2016, he has served on the Steering Committee for the IEEE Transactions on Sustainable Computing. Previously, he was a member of the editorial board of Cluster Computing, the Journal of Networks, Software Tools and Applications (2000 – 2010), and was a Special Issue Editor for the Journal of Parallel and Distributed Computing (2010). He served as an evaluator on the IEEE Computer Society Fellow Evaluation Committee for 2011-2012, and as a vice-chair for the IEEE Fellow Evaluation Committee for 2013, 2016 and 2018. He was appointed to be the 2019 Chair of the IEEE Computer Society Fellow Committee. He has served and continues to serve on the executive and technical program committees of numerous international conferences including: The Optical Society of America, meetings on Optics in Computing, the IEEE/OSA conference on Massively Parallel Processing using Optical Interconnects(MPPOI), the IEEE Symposium on High Performance Computer Architecture (HPCA), the International Symposium on Computer Architecture (ISCA), the International Parallel & Distributed processing Symposium (IPDPS), the International Conference on Parallel and Distributed Computing & Systems (PDCS), the International Conference on Parallel Processing (ICPP), the ACM/IEEE Symposium on Architectures for Networking & Communication Systems (ANCS), the IEEE/ACM International Symposium on Microarchitecture (IEEE Micro), the International Conference on Parallel Architectures & CompilationTechniques (FACT), the ACM/IEEE International Symposium on Networks-on-Chips (NOCS), the IEEE Hot Interconnects (HOT), and the IEEE International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoC), among others. He has served on the panels of several funding agencies and is often invited to be the Keynote Speaker at various conferences.