IP Session 12C: Fault Localization Practices and Challenges
Organizer: Sarveswara Tammali
Texas Instruments (India) Ltd, C.V. Raman Nagar, Bangalore-93, India

1. Current practices of FA Engineer / DFT engineer and Challenges
Sarveswara Tammali* (Texas Instruments, SOC Design, Bangalore, Email: sarvesh@ti.com), Kendal Scott Wills (Texas Instruments, Device Analysis Operations, Houston, USA) and David Paul (Texas Instruments, Device Analysis Operations, Houston, USA)

As the semiconductor industry moves towards devices of higher integration using smaller and denser fabrication techniques, the need to understand failure mechanisms is becoming increasingly crucial. Scan based diagnostics has been touted as the enabler to failure analysis (FA) of these designs. The FA engineer is relying on capability of ATPG tool diagnosis to isolate the defect, to a level of suspect node based on tester log. On the contrary, due to compressed scan patterns introduced by DFT engineer to reduce the test cost, FA is losing its precision to uniquely isolate the defect. Current Design for FA (DFFA) needs to close the gap between need for diagnosability of failure mechanisms of shrinking technologies and required tools, flows, structures in devices necessary to isolate the potential defects to enable corrective action. It should also provide the stimulus to the universe of Fail Site Isolation Techniques. On technologies of 65nm, 45nm and below, generating manufacturing tests targeted to Design for Manufacturability (DFM) violations in the layout in addition to conventional stuck-at and at-speed tests seems to be a suitable approach to achieve the desired test quality, cost and a more robust FA signature. The presentation will initially expose conflicts of FA and DFT requirements and continue with the discussion on the current practices and challenges faced by the FA/DFT engineer to support scan diagnosis to localize the defect that will guide physical failure (PFA) analysis.

2. Principle and Practice of Modern Scan Diagnostics
Scott Cook* (Mentor Graphics, Email: scott_cook@mentor.com) and Brady Benware (Mentor Graphics)

With each new semiconductor technology node, smaller features sizes lead to new classes of defects. Issues such as pattern size, test time, IO pin limitations as well as the need for advanced fault models also require the use of compression for scan based testing. The traditional methods of visual inspection and wafer mapping can take days or even weeks to localize defects on a chip for root cause analysis. This is especially true when using advanced fault models with compression technologies unless the capabilities of current scan diagnostic tools are understood. These new tools look within the die to identify, classify and locate new defect mechanisms. By using scan diagnostics, the localization time (specifying the location of the defect) can be reduced from days or weeks to a matter of hours. This session will outline current scan diagnostic methods for compressed scan and outline how to take advantage of physical layout information to more quickly and accurately identify failure mechanism as well as discuss the direction scan diagnostics will take in the future.

3. Tester-based Scanning Optical Microscope Techniques for Fault Localization
Jacob CH Phang* (SEMICAPS Pte Ltd, Email: phangjch@semicaps.com) and MR Bruce (AMD Inc)

The use of scanned near infra-red (NIR) laser beams to actively localize failures which are sensitive to electron-hole pair generation or thermal stimulation have led to the development of various power alteration techniques for fault localization. A new methodology that integrates test and scanned NIR lasers such as Soft Defect Localization (SDL) has been developed recently. In particular, SDL combines localized laser heating with the pass-fail state of a device to successfully localize soft defects. Subtle, thermally sensitive soft defects can be localized by careful selection of the IC voltage, temperature, and operating frequency. In this presentation, the critical performance parameters for tester-docked scanning optical microscopes in implementing SDL and LADA techniques will be presented. Several case studies to illustrate these applications will also be presented.