Special Session 9B

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The limit of present silicon transistors is set by the manufacturing process and not by the laws of physics. Emerging nanomaterials has provided new possibilities for higher packing density, higher carrier mobilities, and higher/lower dielectric constants. Although nanotechnology is usually defined as utilizing technology with less than 100nm in the minimum feature size, nanoelectronics often refer to devices that are so small that inter-atomic interaction, ballistic transport, and quantum mechanical properties need to be studied. These phenomena are expected to assume much more prominent roles in silicon-based devices fabricated using sub-45 nm technologies.

Nanoelectronic devices such as Single Electron Transistor, Resonant Tunnel Diodes and Quantum Dot Arrays are still under development as practical circuitry, but they do hold a great promise. This is also true of molecular devices that can self-assemble to form a large system. One of the best known families of nanomaterials is carbon nanostructures such as nanotube, nanofiber, and graphene. They hold great promise as candidates for ultra-fast switches as well as interconnect and thermal interface materials. In this session, three speakers will present different facets of nanoelectronics to prepare us test engineers for the challenges integrated circuit technology faces now and in the near future.

1. One Dimensional Nanostructures and their Applications
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Carbon nanotubes exhibit unique electronic properties propelling their use in a variety of applications including electronics. The ability to grow a variety of semiconductor, oxide and other inorganic materials in the form of nanowires with controlled properties and vertical orientation provides a competitive avenue for applications in logic, memory, data storage, sensors and others. This talk will provide an overview of emerging nanotechnology applications of interest to the VLSI community. The author acknowledges contributions from Bin Yu, Jeff Sun, Jing Li, Y. Lu and Jun Li.

2. Emerging Nanoelectronic Devices
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It is predicted that silicon CMOS transistor could be ultimately scaled down to 1.5 nm gate length based on the least energy model for computing. However, it is also anticipated that a gate length of 4-5 nm would be the practical limit. There are device candidates that are of strategic importance beyond the ITRS Roadmap. Some were actively explored in research community for long, while a few others were catching up very rapidly. Of particular importance are nanostructure-based devices that potentially offer unique properties such as scalability, power efficiency, and low material/processing cost, etc. These new technologies, possibly serving as “enablers”, would help the continued advancement of IC chip technology in applications such as information processing and data storage not necessary through traditional geometry scaling. In this talk, some trends will be discussed on the mainstream chip technology in the next one-and-a-half decade towards the “scaling-end” of the Roadmap. The state-of-the-art research in the upfront will be introduced and major challenges will be highlighted.

3. Carbon Nanostructures as On-chip Interconnects
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As integrated circuit (IC) technology continues the trend towards sub-50 nanometer feature sizes, it is imperative to retain performance of back-end features such as on-chip interconnects while gaining the cost benefit of scaling. Some major barriers to achieving continuous downward scaling include high resistance and questionable reliability of nanoscale copper lines, and power dissipation in densely packed integrated circuits. This work presents fundamental electrical characterization of carbon nanofibers (CNF) as a possible solution for next-generation back-end integrated circuit processing. Results of temperature-dependent electrical resistance measurements for CNF arrays demonstrate distinct metallic behavior of these novel nanoscale devices. Microstructural characterization using high-resolution electron microscopy techniques are presented and its implications discussed. In addition, a recent study of the current-carrying capacity of CNF interconnects is presented.