IP Session 7C: Design for Yield and Manufacturability
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Increased manufacturing variability in leading-edge process technologies requires new paradigms and solution technologies for yield optimization. SoC manufacturability and yield entails design-specific optimization of the manufacturing, and thus enhanced communications across the design-manufacturing interface. A wide range of Design-for-Manufacturability (DFM) and Design-for-Yield (DFY) methodologies and tools have been proposed in recent years. Some of these tools are leveraged during back-end design, others are applied post-GDSII, and still others are applied post-design, from reticle enhancement and lithography through wafer sort, packaging, final test and failure analysis. DFY and DFM can dramatically impact the business performance of chip manufacturers. It can also significantly affect age-old chip design flows. Using DFY and DFM solutions is an investment, and choosing the most cost effective one(s) requires careful analysis of integration and schedule overheads, versus quantified benefits. This session analyzes the key trend and challenges, and provides a set of innovative DFM and DFY practices used for today’s SoC designs.

Presenters

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