Critical products like automotive, aerospace and medical demand 0-defect silicon. This Innovative Practices session will address different approaches taken by some of the key semiconductor manufacturers to achieve zero-defects. The three presentations in this session, and their descriptions are given below.

**Title: DFT Opportunities to achieve Zero Defects**  
**Authors:** Rajesh Raina*, LeRoy Winemberg, Freescale Semiconductors, USA  
**Abstract:** Zero Defect (ZD) objective is met today with a comprehensive and inter-disciplinary ZD Program that spans across the entire IC development flow. DFT is a critical component of the ZD Program and has the potential to increase its utility. While Scan and Memory BIST are being used effectively, the DFT methodologies around Analog, RF, MEMs, High-Speed IO and Mixed-Signal logic are not well established. Advances in Low Power design - such as Dynamic Voltage and Frequency Scaling, Power Domains and the use of sophisticated Clock-Gating structures - have created new challenges for testing these Low-Power structures as well as rest of the IC. Finally, for 45nm and below, Yield is a big issue. One of the key requirements for Zero Defects is high Yield. DFT methods have the potential to accelerate Yield Learning for new processes so that they can achieve ZD qualification in a timely manner. This presentation will describe the DFT opportunities, what has been done and a collaborative framework for future work.

**Title: Statistical Scan Diagnosis - new road to high quality**  
**Authors:** Stefan Eichenberger, Camelia Hora, Jeroen Geuzebroek, Bram Kruseman, Ananta K. Majhi*, NXP Semiconductors, Netherlands  
**Abstract:** Yield and quality monitoring in a fab-less environment is challenging, but becoming increasingly more important. With limited information (mainly, scan diagnosis and bitmap) yield limiters need be attributed to defects, parametric variations and design marginalities. Potential quality risks need be screened out efficiently. In this case study, we will show how we identified a potentially quality relevant process issue in a 90nm process. It affected only a handful of dies per lot (amidst a much higher total yield loss). Still, statistical scan diagnosis results in affected areas of the wafer were sufficiently different from results in other areas to enable conclusions about the underlying defect type, and hence a risk assessment. Statistical scan diagnosis – known for yield analysis - is hence entering the realm of quality monitoring.

**Title: Extending Quality Beyond Time Zero Through Additional DFT and Test**  
**Authors:** Srinivas Kumar Vooka, Vinay Jayaram and Rubin Parekhji*, Texas Instruments, Inc.  
**Abstract:** The normal adoption for DFT (design for testability) practices is for improvements in manufacturing test quality. An accepted measure of such quality is time zero defective part escapes measured in defective parts per million (DPPM). With increasing design complexity, higher levels of integration and performance, and more stringent quality requirements in safety critical applications, the quality measures of such designs must extend beyond time zero DPPM based on tests for standard fault models. These include the need to (a) analyse performance schmoos, (b) target defect model coverage, (c) debug and diagnose silicon fails, and (d) execute lifetime tests in the system. DFT is expected to play an increasingly important role in enhancing such forms of test quality. In this presentation, DFT implementation techniques and supporting silicon data will be presented to illustrate how such improvements have been incorporated in some recent designs in Texas Instruments. This will be addressed in multiple areas, namely, (i) design support for periodic field testing, (ii) DFT support for silicon fail debug, (iii) ATPG for at-speed performance tests and defect based testing using small delay defect and other defect models, and (iv) alternate test mechanisms for stress mode testing, and ascertaining their effectiveness.

While these techniques are currently ad-hoc in nature, they are expected to be increasingly used in newer designs. These, in turn, will also drive additional design, DFT and ATPG practices for adaptive testing, wherein design and test adaptivity are important to meet various test quality requirements. For example, a different collection of existing tests will be required to be applied at different times, and the quality measures for such test application will be correspondingly different. Lifetime tests can help to ascertain field DPPM, stress tests can ascertain reliability DPPM, and performance tests can ascertain variability DPPM. This presentation will also highlight how DFT can be used to impact such quality measures as well.