Getting Started with VHDL

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Abstract
This paper describes a module developed by the author for the initial teaching of VHDL. A ‘self-teach’ approach is adopted whereby students with a minimum of tutor support can progress from a basic knowledge of digital logic to modelling an ALU in six three hour sessions. The course script and its accompanying assessment manual are written in such a way as to be portable and easily updated. Evaluation following three successful years of delivery has shown that this introduction provides a sound basis for more advanced work. Copies of the script and the supporting source code can be obtained from the author.

1. Introduction

“Getting started with VHDL” is a first-year introduction to VHDL designed to be taken by students on a specialist 3-year undergraduate degree programme entitled Electronic Systems Engineering. The focus of this programme is on digital systems and VLSI design and it attracts between 10 and 20 students per year. It differs significantly from other degree programmes offered by the Division by having a fast-track digital systems design course in year 1 followed in year 2 by a VLSI project to be completed in final year. The aim of the programme is to develop the students’ ability to implement complex electronic systems

VHDL is the cornerstone of all design activities throughout the second and third years of the programme. The expressiveness of VHDL lends itself well to specification of system behaviour and to subsequent design decomposition to synthesizable units for implementation. Proficiency in VHDL must therefore be achieved as early as possible in the curriculum. Because of the many calls on the time available for formal teaching through lectures and seminars it was decided that a different approach was desirable for VHDL. Past experience in teaching conventional programming languages had shown that students achieve more if allowed to adopt a self-paced learning style. Thus, the VHDL module described in this paper is normally completed in six self-paced 3-hour laboratory sessions but of course students are permitted to spend extra time if they need it. The learning process is based primarily on a course script and workbook. However during scheduled laboratory sessions extra support is available from a postgraduate teaching assistant and at other times from a PC based multimedia tutorial [1]. Once established, the module has required very little staff effort to maintain and has been very well received by students. The students work in a Mentor Graphics environment on HP workstations but the course script has however been designed to be easily adaptable to any CAD environment.

2. Module content

The approach taken throughout the script is to provide an illustration of how a particular behaviour can be modelled in VHDL and then to set a problem to reinforce understanding. Feedback on success or otherwise is given immediately by the teaching assistant referring as necessary to the assessment manual provided. At the start of the course a basic knowledge of simple gate level design is assumed. Thus, by writing VHDL for simple gates, multiplexors and adders the student gains a rapid understanding of entities, architectures and components in behavioural descriptions. Data types are gradually introduced together with packages to model increasingly complex functions. This leads on to examples of how VHDL handles concurrent and sequential systems. Finally the students encounter enumerated types and test benches.

The module does not follow the syntactic approach taken by most text books on VHDL. Although such text
books are excellent as reference sources they are considered too expensive by undergraduates and difficult to follow. Instead the example-driven approach taken by the module is preferred because it relates much more closely to the design methods taught in lectures. The module content is summarised as follows.

- Why VHDL?
- The entity and architecture
- Ports and signals
- Data types and packages
- Multivalued logic
- The process
- Sequential statements
- Delta delays
- Variables and signals
- Enumerated types
- Test benches

The examples covered range from simple gates to an ALU.

3. Assessment

Since the objective of the module is for a majority of students to achieve competence in writing VHDL, it is not considered sufficient simply to base marks on working code. The assessment manual thus requires the tutor to reward good style and structure and to give credit to success achieved with a minimum of external help.

4. Conclusions

The module is in its third year of use. It has been significantly improved as a result of student feedback and as a preparation for future advanced work using VHDL it appears to have no shortcomings. On completion students have developed sufficient confidence inspired by the ‘self-teach’ approach to tackle sophisticated modelling problems on their own.

Maintenance effort is low and student satisfaction is high, both at the time and when viewed in retrospect in later years where VHDL forms the basis of project work.

Copies of the course text as a WORD document can be obtained from the author.

Reference

1. Multimedia VHDL Tutorial, Esperan Limited, Unit 1, Hilldrop Lane, Ramsbury, Wiltshire, SN8 2RB, England.