Advances in process technology have enabled integrated circuits to approximately double in complexity every year. Today's VLSI circuits are approaching 500,000 transistors; and we envision 5 and 50 million device circuits in the not too distant future. While process technology has driven the increase in circuit complexity, the design tools have lagged behind and constrained the designer. Even with the rapidly accumulating knowledge of VLSI design, the time required to design, layout and test VLSI circuits is growing linearly with the complexity of the circuits. New tools, oriented toward dramatically increasing productivity, are necessary to avoid design catastrophe.

Computers have assisted IC designers for the last ten years. Mainframes, located in remote computer centers, are used to run logic simulators such as TEGAS and circuit simulators such as SPICE. CAD systems, located in special rooms and operated by trained technicians, are used to capture the graphical data depicting the layout of the design. Other mainframes are used to run design and electrical rule checking programs. Extensive CAD departments have been established to manage the people and computers as well as integrate the various software programs.

This environment isolates the design groups. Logic and circuit designers create the schematics and layout engineers working in the CAD group execute the physical design. Communication between these groups is often paper based, and hand-drafted schematics and design plots easily get out of date. Manually generated netlists take many hours to debug. Simulation response time on time-shared computers discourages use. Multi-user layout systems become agonizingly slow just when the design crunch comes. Layout verification, run in batch mode on mainframes, requires time consuming data translation and data transfer. Designers may have to wait a day or longer for turn around on even an LSI circuit.

The engineering workstation gives the VLSI designer a superior work environment. Complete integration of the tools for each stage of the design process minimizes data translation and transfer. Powerful 32-bit workstations with multi-megabyte memory ensure each designer has the performance and capacity to handle VLSI circuits. Advanced virtual access networking schemes tie the design groups together with a single network-wide database. Sharing data and distributing designs among a large development team is easy and efficient. Layout technicians have immediate access to the latest schematics, and circuit designers have immediate access to the most recent layout data.

Hierarchical design capture tools assist in the structuring and management of complex designs. Hardware accelerators give the designer the performance and capacity to handle large logic simulations. Advanced circuit simulators, like the Simon Simulator, take a giant leap forward in circuit simulation capability. Spice, the workhorse of circuit simulation, has limitations in execution speed, circuit size, and user friendliness. Mentor Graphics pioneered graphical user interfaces with the MSPIECE simulator. Having added a unique interactive capability to standard Spice and now to the Simon Simulator, the designer can view and probe the schematic as if probing a breadboard while running the simulator. The MSIMON simulator offers dramatic performance improvement over standard Spice (up to 50x) while maintaining SPICE compatibility. With the MSIMON simulator running on a powerful workstation the designer has the performance and capacity to simulate very large MOS circuits.

Advanced layout editors speed the design capture process as well as insuring that the design data is entered accurately. Boolean editing functions facilitate creating complex geometric shapes. Interactive design rule checking helps insure that the data is entered correctly - BEFORE the errors are propagated throughout the design. By obtaining quick feedback on the accuracy of the design and by eliminating the time consuming data translation and transfer time for batch design rule checking, the VLSI designer can cut the overall development cycle. The DRACULA II layout verification system executing on CHIP STATIONS' powerful 32-bit processor enables the designer to complete the full suite of DRC, ERC, and network consistency checks on the local workstation. This gives the designer complete control of the VLSI design process and eliminates the time consuming data transfer to a mainframe computer.

Multi-window editing environments give the designer an easy way to execute cross chip edits and move around the layout quickly. On-screen access to a single network-wide schematic ensures the designer is aware of the latest revisions. User definable menus and macros give the designer the flexibility to customize the system to any particular design style.

True hierarchical design techniques will become more important as VLSI circuits increase in complexity. Object-oriented VLSI design, where the specification of a module is separate from the implementation of the module facilitates partitioning and simplifies assembly. The CHIPGRAPH layout editor supports hierarchical design with its separation of a cell's external interface and the cells internal description.

By integrating all stages of the design cycle, delivering simulation tools with the capacity and performance for VLSI circuits, and incorporating layout tools that speed data entry and verification, the engineering workstation has become reality for the VLSI designer.