Making the most of VLSI in microcomputers

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ABSTRACT

An introduction to the innovative SCAT design philosophy for VLSI microcomputers of Texas Instruments (TI) is presented. The recently announced 8-bit TMS7000 Microcomputer family is used as an example of a SCAT design. TMS7000 benefits resulting from SCAT include a very dense bar for lower chip costs and microcomputer prices; a unique microprogrammability feature that will allow a user to modify the instruction set for the few applications that require it; and the architectural flexibility that will allow TI to bring many new microcomputer devices to the marketplace quickly and easily.
THE MICROCOMPUTER LAYOUT PROBLEM

Design techniques for large-scale integrated microcomputer circuits have traditionally followed those of printed circuits. Separate design teams typically pack desired functional performance into separate functional blocks. The job of interconnecting the functional blocks is left as the last step.

Thus, in comparison with memory chips, microcomputer designs tend to sprawl over large areas of silicon. As the complexity of microcomputers has increased, the interconnections between the various subunits can consume a significant portion of the available silicon. If random logic is used, its irregularity makes the problem worse.

SCAT ARCHITECTURE

Texas Instruments made an important step toward moving microcomputer design into the VLSI era with the introduction of the Strip Chip Architectural Topology (SCAT). SCAT integrates architecture and layout into a dense, memorylike, array-structured chip. SCAT replaces as much random logic as possible with regular structures such as read-only memories (ROM) and transistor arrays. TI's recently announced TMS7000 family of single chip, 8-bit microcomputers represents the culmination of the SCAT design philosophy.

With SCAT, the chip's layout is not left until the end of the design process, but is an integral part of it. For example, the TMS7000's registers for the timer, I/O control interrupt handling, and arithmetic logic unit are arranged in a strip. The chip appears to be a tightly stacked set of 8-bit-wide bricks that are interconnected through a data bus (see Figure 1).

Since the memory-intensive subunits are aligned in vertical strips, practically all the interconnection paths run over silicon that has already been used for active devices. The polysilicon and metal interconnections are made with an absolute minimum of signal path length, which also lessens the required size for the line drivers.

The net result of TI's SCAT is a very powerful microcomputer packed into a small chip size. The 2K ROM TMS7020 microcomputer, for example, has a chip area of 35,000 square mil using conservative 4.5 micrometer design rules that can easily be shrunk to 3.0 μm rules.

The costs of fabricating a microcomputer chip are exponentially related to chip size. For example, a microcomputer chip with only a 10% increase in silicon area (with the same design rules) could cost up to twice as much to manufacture! Small microcomputer chips equate to lower chip costs and thus to lower pricing to microcomputer customers.

MICROPROGRAMMABILITY

To take advantage of the silicon efficiency of ROM over random logic, TI replaced the traditional programmed logic array and associated random logic with a Control ROM to implement internal control of the TMS7000 microcomputer. The Control ROM stores the microcode that determines the instruction execution sequence.

Microcoding of the TMS7000 is extremely simple because of the general technique of instruction decode. The CPU has no microprogram counter; instead, the present Control ROM state supplies the address of the next state. With microprogramming, all the necessary control signals are contained in a single microinstruction lying lengthwise down the Control ROM. No complex routing or combinational logic is required. Most instructions executed by the TMS7000 share microstates with other instructions. This simple microarchitecture and microcode-sharing technique result in a reduced chip size while increasing tremendously the flexibility of the TMS7000.

Probably the single most unusual feature of the TMS7000 is the flexibility the microprogramming feature offers the customer. The already powerful standard TMS7000 instruction set can be altered or customized for applications that require unique performance, memory, or I/O features. These user-defined instructions are substituted for standard TMS7000 instructions on the Control ROM.

In some user applications, microprogramming will enhance TMS7000 performance. By combining or modifying the existing microinstruction execution sequence to perform critical tasks or subroutines in less instruction clock cycles, the throughput or "speed" of the TMS7000 in the user's application is enhanced.

Another advantage to microprogramming is that in specific applications it can allow more efficient use of the limited on-chip program memory. By combining or modifying the standard microinstruction execution sequence for unique repetitive tasks or subroutines, the total overall application program may require fewer steps and less on-chip program memory.

In effect, microprogramming can be also thought of as a safety net for the design engineer should he/she overestimate his/her software capability or underestimate the application system requirements.

Microprogramming could also be useful in providing increased system security for TMS7000 customers competing in very competitive business environments. Reverse engineering of a system implemented on a TMS7000 microcomputer with a unique user-defined instruction set would be difficult.

ARCHITECTURAL FLEXIBILITY

Because of the unique structure of the SCAT design philosophy, the orthogonal control and data paths are readily available to modify or enhance the TMS7000 chip.
For example, TI created the TMS7040 4K ROM version from the 2K TMS7020 2K ROM version without redesigning the chip. The chip design was separated at the memory border, and the additional 2K of memory was singly inserted by the design computer. Likewise, additional features such as more ROM, RAM, or different I/O structures can be added with a minimum of design resources and time.

TI plans to take advantage of SCAT by adding many device members to the TMS7000 family in the near future. EPROM, CMOS, communications devices, and more are in design.