High-performance, high-capacity single-chip microcomputers

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ABSTRACT

The MC6801 Single-Chip Microcomputer has long been recognized as a high-performance microcomputer. This paper provides a brief look at the complete M6801 family and then discusses the enhancements made to the Timer and Serial Communications Interface circuitry of the basic MC6801 to develop the new MC6801U4 microcomputer.

The MC6801U4 strengthens the M6801 family position in the high-performance single-chip microcomputer marketplace.
INTRODUCTION

The past several years have brought about expanded markets for Single-Chip Microcomputers (MCUs). Some of these new markets are demanding higher-performance MCUs for future products. Higher performance does not mean merely an internal memory map expansion; it also means improved features and functions, along with versatility in application.

Requirements in industrial control, communications, automotive, and many other such applications are constantly demanding higher-performance MCUs.

The M6801 family has met this high-performance and versatility need and continues to improve as its product portfolio grows. The M6801 family follows the compatible evolutionary expansion that was established throughout the development of the M6800-based microprocessor family.

Table I shows the products in the current M6801 family and the basic features associated with each member.

VERSATILITY

The M6801 family has the ability to operate in two worlds—as a microcomputer or as a microprocessor. The fundamental operating modes of the members in the M6801 family products are these:

1. Single-chip
2. Expanded nonmultiplexed
3. Expanded multiplexed

Within these fundamental operating modes the resources of the microcomputer are briefly summarized in the following paragraphs and allocated as shown in Figure 1.

Single-Chip

In the single-chip operating mode the MC6801 operates with all internal memory resources. This operating mode makes maximum use of the input/output capabilities with no address or data buses.

Expanded Nonmultiplexed

The expanded nonmultiplexed operating mode uses internal memory resources and allows the modest increase of 256 bytes of read/write locations. This mode uses separate data and address buses, thereby reducing the number of input/output functions available.

Expanded Multiplexed

The expanded multiplexed operating mode removes some or all of the internal memory resources and allows the MC6801 to function as a high-performance microprocessor. In this mode the external address space can be expanded up to 64K bytes for external resources.

THE ENHANCED FAMILY ANSWER

The M6801 family is continuously growing. The latest member is the MC6801U4, which is an enhanced MC6801 that is pin- and object-code-compatible. All addressing modes and features of the MC6801 remain intact. The enhancements are increased ROM, increased RAM, and improved Timer and Serial Communications Interface circuitry.

Where the additional features of the MC6801U4 require additional input/output, more of the port pins have been made multifunctional, as shown in Figure 2.

The internal ROM of the MC6801U4 has been doubled in size, from 2048 bytes to 4096 bytes. The interrupt vector locations are maintained as in the MC6801 for compatibility.

The internal RAM has been increased from 128 bytes to 192 bytes. The standby RAM portion of this memory has been decreased from 64 bytes to 32 bytes. This decreases the amount of standby current required to maintain the memory contents during power down.

### TABLE I—The M6801 family

<table>
<thead>
<tr>
<th>Feature</th>
<th>6801</th>
<th>6803</th>
<th>6801U4</th>
<th>6803E</th>
<th>6803U4</th>
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<tbody>
<tr>
<td>ROM size</td>
<td>2K bytes</td>
<td>—</td>
<td>4K bytes</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>EPROM size</td>
<td>—</td>
<td>2K bytes</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>RAM size</td>
<td>128 bytes</td>
<td>128 bytes</td>
<td>192 bytes</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>Stdby RAM size</td>
<td>64 bytes</td>
<td>64 bytes</td>
<td>32 bytes</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>I/O lines</td>
<td>29 I/O 2 ctrl</td>
<td>29 I/O 3 ctrl</td>
<td>29 I/O 2 ctrl</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>Timer</td>
<td>16-bit/3 funct</td>
<td>16-bit/3 funct</td>
<td>16-bit/6 funct</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>SCI/baud rates</td>
<td>Full/4 selec</td>
<td>Full/4 selec</td>
<td>Full/8 selec</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>RAM size</td>
<td>—</td>
<td>128 bytes</td>
<td>128 bytes</td>
<td>192 bytes</td>
</tr>
<tr>
<td></td>
<td>Stdby RAM size</td>
<td>—</td>
<td>64 bytes</td>
<td>64 bytes</td>
<td>32 bytes</td>
</tr>
<tr>
<td></td>
<td>I/O lines</td>
<td>—</td>
<td>29 I/O 2 ctrl</td>
<td>29 I/O 2 ctrl</td>
<td>29 I/O 2 ctrl</td>
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<tr>
<td></td>
<td>Timer</td>
<td>—</td>
<td>16-bit/3 funct</td>
<td>16-bit/3 funct</td>
<td>16-bit/6 funct</td>
</tr>
<tr>
<td></td>
<td>SCI/baud rates</td>
<td>—</td>
<td>Full/4 selec</td>
<td>Full/4 selec</td>
<td>Full/8 selec</td>
</tr>
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</table>
Single-Chip (Mode 7)
128 bytes of RAM; 2048 bytes of ROM
Port 3 is a parallel I/O port with two control lines
Port 4 is a parallel I/O port

Expanded Non-Multiplexed (Mode 5)
128 bytes of RAM; 2048 bytes of ROM
256 bytes of external memory space
Port 3 is 8-bit data bus
Port 4 is an input port/address bus

Expanded Multiplexed (Modes 0,1,2,3,6)
Four memory space options, (total 64K address space)
(1) Internal RAM and ROM (Mode 1)
(2) Internal RAM no ROM (Mode 2)
(3) No Internal RAM or ROM (Mode 3)
(4) Internal RAM, ROM with partial address bus (Mode 6)
Port 3 is multiplexed address/data bus
Port 4 is address bus (inputs/address in Mode 6)
Test Mode (Mode 0):
May be used to test internal RAM and ROM
May be used to test Ports 3 and 4 as I/O ports
Any mode can be irreversibly entered from Mode 0

Resources Common to all Modes:
Reserved Register Area
Port 1 Input/Output Operation
Port 2 Input/Output Operation
Timer Operation
Serial Communications Interface Operation

Figure 1—Summary of M6801 fundamental operating mode resources

TIMER
The timer features and registers of the MC6801 have been maintained and expanded. Three additional registers have been added, along with an additional input capture register and two additional output compare registers. Figure 3 is a basic block diagram of the MC6801U4 timer circuitry.

Dual Counter Register
The MC6801U4 has a duplicate timer control register. This Dual Counter Register allows software to examine the counter without the resetting of the Timer Overflow Flag in the Timer Control and Status Register.

Timer Control Register 1
A second counter register has been added, Timer Control 1, which allows the MC6801U4 to control the states of the pins associated with the output compare and input capture registers.

Timer Control Register 2
Timer Control 2 has been added for handling timer interrupts from the output compare and input capture registers. This allows software testing of the timer counter without clearing any of the associated status bits.

Input Capture Registers
A second input capture register has been added. The two input capture registers can be programmed independently to take a “snapshot” of the timer counter register at an appropriate transition on their associated input pin.

Output Compare Registers
The output compare feature has been extended by adding two additional output compare registers. These three registers can be programmed independently to respond to a match in the counter register and cause an appropriate transition on the associated output pin.

Serial Communications Interface
All the serial communications interface functions remain identical to those of the MC6801, and four more baud rates have been added. Table II shows the baud rates available for three given crystal frequencies.

SUMMARY
The MC6801 has been a leader among the available high-performance microcomputers in the marketplace for several years. The MC6801 continues to gain momentum in control and processing applications.
The enhancements added to the newest member of the family, the MC6801U4, allow the momentum already established by the existing MC6801 family of products to continue.
Diverse applications will continue to demand more and more powerful microcomputers. The MC6801 family products demonstrate that they are able to meet the challenge.
Figure 2—MC6801U4 8-bit microcomputer-block diagram

Figure 3—MC6801U4 timer-block diagram

TABLE II—SCI bit times and rates

<table>
<thead>
<tr>
<th>EBE</th>
<th>SS1:SS0</th>
<th>E</th>
<th>Baud</th>
<th>Baud</th>
<th>Baud</th>
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<tr>
<td>0</td>
<td>0</td>
<td>16</td>
<td>38400.0</td>
<td>62500.0</td>
<td>76800.0</td>
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<tr>
<td>0</td>
<td>0</td>
<td>128</td>
<td>4800.0</td>
<td>7812.5</td>
<td>9600.0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1024</td>
<td>600.0</td>
<td>976.6</td>
<td>1200.0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>4096</td>
<td>150.0</td>
<td>244.1</td>
<td>300.0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>64</td>
<td>9600.0</td>
<td>15625.0</td>
<td>19200.0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>256</td>
<td>2400.0</td>
<td>3906.3</td>
<td>4800.0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>512</td>
<td>1200.0</td>
<td>1953.1</td>
<td>2400.0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>2048</td>
<td>300.0</td>
<td>488.3</td>
<td>600.0</td>
</tr>
</tbody>
</table>

*Using maximum clock rate

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