INTRODUCTION

The concept of standardization and the advantages which it offered by-passed the semiconductor memory industry for the first five years of its existence. Standardization has never been easy to achieve in the modern electronics industry, but it has been doubly difficult for the fledgling semiconductor memory industry.

This difficulty can probably be attributed to the highly competitive nature of the industry combined with the high technology levels involved in the products. Each company had what they felt were advanced proprietary concepts, processes, and designs. This, they felt, would give them a competitive edge so they were reluctant to talk to the competition regarding standards, for fear that they might lose some of their commercial advantage.

The lack of standardization extended over a broad range of aspects of the industry. The language used by each company in describing its product was different from that used by its competitors, even when the products were intended to be interchangeable.

Beyond the lack of communications standards, there was the more fundamental problem that the product images and characteristics were not standardized. At one time there were over four different 1K dynamic MOS RAMS. The situation got worse with the advent of the 4K dynamic RAM. At least seven different noninterchangeable designs were announced, each described in a different language.

The first 4K devices to be introduced were in a 22 pin package. The twelve address bits were supplied in parallel. From a performance standpoint, the parts were generally compatible. However, the two companies which led the field chose to use different pinouts, making the parts incompatible. In addition, a third company introduced a part which was compatible with one of these except that the output was different. It had a low level constant current rather than a TLL compatible voltage out.

Following the original 22 pin devices, there were three different 18 and 16 pin devices introduced. The two 18 pin devices used different pin-outs and interface logic. The 16 pin design used a two clock, multiplexed address interface logic.

In addition to the gross differences of pin-out and logic, there were numerous cases of subtle differences in timing requirements and interface signal levels which created incompatibilities between parts.

Another aspect of Semiconductor Memory where we have been hampered by the lack of standards is related to device test. A critical aspect of testing is the test pattern used. This is the address and data sequence which when combined with the power supply voltages and interface voltages and timing, are used to determine if a device meets specifications or not. Often, in marginal devices, minor variations in the test pattern can make the difference between detecting a bad part or not. It is essential that we be able to communicate the exact details of these test patterns so that tests may be duplicated by vendors and customers.

Several years ago, a group of engineers representing both vendors and users recognized the problems which resulted from this lack of standards and set off to correct the situation. They formed a committee and then petitioned the IEEE Computer Standards Committee to sponsor their work. The group became formally recognized as the "Semiconductor Memory Standards" sub-committee. The membership is made up of representatives from device manufacturers, manufacturers of computers and related equipment, and memory test equipment manufacturers.

The group normally meets twice a year at the solid state circuits conference in February and at the semiconductor memory test symposium in October.

The sub-committee is made up of several task groups which meet more frequently to prepare drafts of standards to present to the sub-committee. At the present time there are three task groups working on standards. The first of these is working on standards related to the electrical description of Semiconductor Memory devices. The second group has addressed the problem of describing the test pattern used to test Semiconductor Memory devices. The third one, which is now being organized, will develop technical standards for describing and measuring the thermal properties of memories and other integrated circuits.

STANDARDS IN PROCESS

There are three standards currently in various stages of preparation. The first one is being developed by the device description task group: It is entitled "Proposed Standard for
Semiconductor Memory Data Sheet Generation. The intent of this standard is to provide a common language and format for the industry to use in describing the electrical and mechanical properties of Semiconductor Memory devices.

The document is divided into four sections. The first section titled "Product Description" lists a series of different items of a general nature which should be included in the specification of any product. It also gives some definitions and logic conventions which are recommended to be used so that the data sheets and specifications can easily be understood by everyone.

Section two, "Product Specification" gives recommendations for the actual electrical and mechanical specifications of the device. In the various sections, ground rules, definitions, and conventions to be used are given. For example, it contains a statement which gives a common definition of the basis for generating the "Absolute Maximum Ratings" section. In the past, there was never a definition of what this means. Every company had its own ground rules for generating these numbers, or in some cases, no ground rules. As a result, the numbers are often arbitrarily chosen and therefore meaningless.

In other areas, definitions and conventions are given to standardize symbology and the presentation of the data. The section on timing specifications is one which has suffered from the largest differences from vendor to vendor and as a result, the greatest amount of confusion amongst the users. The timing specification of current dynamic MOS memory devices is extremely complex. There are typically seven different signals or groups of signals, each of which have up to four critical timing events. Each of these events must be specified with respect to at least one other signal and often with respect to three or four others. The result is a timing specification which often contains a table of over 30 parameters with either a minimum or a maximum value, and sometimes both. For this standard, the task group has invented a symbology and procedure for generating timing parameters to relate any timing event to any other timing event. The result is a uniform, nonambiguous "language" for the timing specification. A summary of the new symbol procedure is included in Appendix A.

In a similar, though less complex way, the voltage and current portions of the specification are covered. Preferred symbols are given for the different lines as a function of their use within the device.

The third section covers the area of use related information. It includes recommendations for the inclusion of information which will simplify the users task of applying the device. The items covered are: graphs showing the interaction between operating variables, current waveforms, bit maps, equivalent interface circuits, testing information, and application information.

The standard is concluded with a series of appendices which give: (1) a summary of input/output pin names, their symbolism and definitions, (2) a format and example of timing specification for a part using the conventions of the standard, and (3) a summary of the timing parameter symbol procedure.

The second standard being worked on is one relating to the description of test patterns for RAM Memory. The original intent of the task group was to accomplish two tasks. The first was to develop a language which could be used to uniquely define the address and data sequence used in a memory test pattern. The second was to use the results of the first task to stabilize the definition of some of the more commonly used patterns such as march, galpat and walking /0.

One of the original ground rules for the language development was that it should be machine independent and not rely on the readers knowledge of the programming language or architecture of any of the currently popular memory testers. The reason for this is the wide disparity between tester pattern generators used. Some work with an absolute address scheme and others use relative addressing. Some define data as a simple sequential string of bits, while others define data as a spacial function of the addresses, while at least one has the capability of doing both.

In its initial efforts, the task group attempted to apply one of the more widely understood high level programming languages, such as APL or Basic. As the standard went through successive drafts, the language evolved into one which tends to be closer to the language of some of the testers. It is undergoing further refinements to satisfy the objections of some of the more hardware oriented sub-committee members.

When the language is stabilized, the task group will then start to develop a repertoire of test patterns which are in common use in the industry. This is being done, not to give support to any patterns as more effective than others, but to improve communications so that when someone uses a pattern name, everyone knows exactly what he means.

The third standard is one which is concerned with the thermal resistance of an integrated circuit. In the past, the terms, symbols, and definitions for I.C. thermal resistance have not been standardized at all. Each vendor and user tends to have his own private set. In addition, some of the definitions used by device manufacturers have no real value to the user in the environment in which he uses the parts.

The work has progressed to the point of having a first draft which has been circulated to the task group for discussion. It will be at least late 1978 before it has been refined to the point where it is ready for presentation to the sub-committee.

The draft standard starts with a series of thermal resistance definitions. The list includes the traditional parameters $R_{th}$ and $R_{thc}$, which are favored by the device manufacturers. It also contains several new ones which allow the user to predict or measure the I.C. junction temperatures under system operating conditions.

The definitions are followed by a section on test methods for measuring thermal resistance. It includes discussions on test fixtures, test devices, test instruments and procedures.

The end result of this effort will be an all inclusive standard which serves the needs of device designers, manufacturers, and users. At the present time, there is no applicable standard for anyone, only a variety of sometimes conflicting traditions.

The work of the sub-committee will continue until those
topics which are the proper province of the IEEE have been considered.

OTHER STANDARDS WORK

There is another class of standards which is badly needed by the industry but which is not properly handled by an organization like the IEEE. This is the standardization of the interface image and specifications of the memory devices themselves. It was this lack of standards which allowed four different 1K devices and seven different 4K devices to be introduced into the market. There is, however, a committee which has been formed, to address this problem. This committee was formed by JEDEC (Joint Electron Devices Engineering Council) as committee JC-42. This committee is made up of representatives of device manufacturers only, however, there is close communication between the IEEE Semiconductor Memory Standards sub-committee and JC-42 so the users voice is well represented.

In addition to the work of JC-42, there are some additional standards work being pursued by other groups. The JEDEC committee JC-11 is preparing standards on the mechanical packages used to house memory devices. Some of the smaller “chip carrier” packages which are now being considered by this committee can have a long range effect on memory architecture. This can come about as a result of the increased packaging density which the use of these packages will allow. In addition, their use opens up the possibility of cost effective multi-chip packages with higher levels of complexity.

There are numerous standards being generated by the N. B. S. or through the MIL specification channels which relate to the Semiconductor Memory field. They are broad based standards which are intended to cover the general field of integrated circuits. One of these is worth noting since it covers topics being considered in the IEEE thermal resistance standard. This work, done by G.E., has been published in the report RADC-TR-77-321, “Thermal Resistance of Microelectronic Packages.”

This is an excellent piece of work which covers in a broad way definitions and test methods relating to package thermal resistance. The work of the IEEE committee is an expansion of this work to make it more broadly useful to the commercial users of integrated circuits.

CONCLUSION

The Semiconductor Memory industry has suffered for its lack of standards. The result has been a needless waste of resources, both by the vendors as well as the users. The progress of the industry has been retarded in ways which it is impossible to quantify. The task of making up this lack has now been undertaken by two separate groups: (1) an IEEE Committee working on standards related to communication and definitions, and (2) A JEDEC Committee working to standardize product definitions and images. The combined results of these committees will greatly assist the Semiconductor Memory industry to develop new, better products and the users to apply them more effectively.
SYMBOLS AND ABBREVIATIONS

This data sheet uses a new type of specification nomenclature that is derived from background work of several users and manufacturers of semiconductor memories. It should help to clarify signal and parameter symbols and definitions and make data sheet information more consistent.

ELECTRICAL PARAMETER ABBREVIATIONS

All abbreviations use upper case letters with no subscripts. The initial symbol is one of these four characters:

- V (Voltage)
- I (Current)
- P (Power)
- C (Capacitance)

The second letter specifies input (I) or output (O), and the third letter indicates the high (H), low (L) or off (Z) state of the pin during measurement. Examples:

- \( V_{OH} \) = Output high voltage
- \( I_{IL} \) = Input low current
- \( I_{0Z} \) = Output off current (leakage)

TIMING PARAMETER ABBREVIATIONS

All timing abbreviations use upper case characters with no subscripts. The initial character is always T and is followed by four descriptors. These characters specify two signal points arranged in a ‘from-to’ sequence that define a timing interval. The two descriptors for each signal point specify the signal name and the signal transitions. Thus the format is:

\[
T_{signal\ name\ from\ which\ interval\ is\ defined\ }^{transition\ direction\ for\ first\ signal}_{signal\ name\ to\ which\ interval\ is\ defined\ }^{transition\ direction\ for\ second\ signal}
\]

Example:

The drawing shows the address setup time defined as TAVEL, Address Valid to Enable Low time.

The signal definitions used in this data sheet are:

- A = Address
- D = Data In
- Q = Data Out
- W = Write Enable
- E = Chip Enable

The transition definitions used in this data sheet are:

- H = transition to high
- L = transition to low
- V = transition to valid
- X = transition to invalid or don't care
- Z = transition to off (high impedance)

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WAVEFORMS

- Waveform symbol must be valid
- Input will be valid
- Change from H to L
- Input will change from H to L
- Change from L to H
- Output will change from L to H
- Don't care: any change permitted
- Changing state unknown
- High impedance