A method for the automatic wiring of LSI chips

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INTRODUCTION

The best known technique for finding a connection between two points is the Moore-Lee algorithm. It is general and thorough, but leads to a long running time. Hightower devised a line-probe wiring scheme which is much more efficient in finding such paths. Variants of this algorithm are probably the most popular means of wiring printed circuit boards at present. However, both of the above techniques suffer from a tendency for the last connections attempted to be blocked unnecessarily by previously wired ones. A more tentative approach to these connections was developed by Hitchcock, whose cellular mazerunner specified connections through cells without fixing their exact location until the end. Schemes which we call line packers for assigning routes to parallel channels have been devised by Hashimoto and Stevens and Kernighan, Schweikert and Persky.

The method described in this paper was motivated by a similar desire to defer final channel selection as long as possible and to give each connection equal treatment. The method consists of subdividing the wiring space into blocks in a hierarchical fashion, assigning connections to block boundaries by perturbing a global trial solution, mapping the solution to a finer grid and eventually allocating wire segments to channels in the vertical and horizontal directions by linepacking techniques.

The results of an implementation of this method, using a two level hierarchy, have proven very successful in production use at IBM.

THE WIRING PROBLEM

The integrated circuit chip consists of a planar array of devices whose logic terminals (pins) are to be interconnected by metal according to a functional specification. The metal lines are made on two layers separated by an insulating material. In order to maximize wiring efficiency, the horizontal segments of a connection are made primarily on one plane (the horizontal plane) and the vertical segments primarily on the other (the vertical plane). The wiring channels on these planes are organized into horizontal streets and vertical avenues (Figure 1).

In this paper, a net is taken to mean a set of pins which are to be connected by metal wires or those wires themselves. A connection is a pair of pins which are to be interconnected, or the metal path between these pins. A segment is a portion of a net which exists within one street or avenue.

Changing planes can be accomplished by introducing via holes in the insulator between the two planes. These vias are made as needed and are not limited to the fixed patterns typical of printed circuit boards.

HIERARCHICAL GLOBAL WIRING

In the first phase of wiring, the chip is divided into a rectangular array of blocks each of which contains many wiring channels and circuit pins. A straight line segment separating adjacent blocks is called an edge. The function of global wiring is to decide which edges the global nets will cross. Nets whose pins are contained wholly within one block (local nets) are not routed at this phase. For large chips, each block can be subdivided after one stage of global wiring into smaller blocks, and the global solution can be further refined (Figure 2).

Each edge can accommodate a number of crossing wires. This is called the channel capacity of the edge and is largely determined by the number of wiring channels crossed by the edge. Each block is assigned an internal capacity reflecting the ease of wiring past the internal nets or other obstacles within the block. The goal of global wiring is to avoid wiring more nets through blocks or edges than permitted by the available capacities.

PERTUBRATION OF A TRIAL SOLUTION

The global wiring can be done, in principle, by any of the traditional mazerunning or line-probe techniques. An essential advance, however, was made by K. A. Chen and later by J. Lee, which we will call wiring by perturbation from a trial solution. The initial trial solution is built up by wiring each net independently. This results in an invalid solution where some regions are over-congested in the sense that wiring demand exceeds edge and block capacity. Nonetheless, this initial solution resembles the real solution much more closely than does a blank wiring image. In addition, the initial solution has the satisfying property of treating all the nets equally.
The net configurations, which can be used to build the initial solution, vary widely: minimum spanning trees, Steiner trees, biased Steiner trees, chains, source of sink trees, and redundant graphs, such as J. Lee's enclosing grid (Figure 3).

The perturbation consists of moving nets or segments away from congestion peaks. This rerouting can be accomplished by mazerunning, parallel translation of segments or by the deletion of redundant segments. In each case, a net or segment is identified as crossing a congested region and then rerouted in a less congested area at the possible expense of increasing its length.

An illustration of this global wiring procedure on an array of 3x3 blocks is given in Figures 4-8. Each number in Figure 4 represents a pin of a circuit. The same numbers on the chip are to be connected to form nets. All the nets are connected in a Steiner fashion without reference to each other. The initial global solution in Figure 5 is, in general, over congested at some boundaries. The number of nets crossing from one block to another is defined as the channel demand at the boundary between the two blocks (Figure 6). Where channel demand exceeds capacity, as outlined in Figure 7, there is clearly a need for rerouting some nets.

The reduction of congestion starts at the worst boundaries. Each net crossing the congested boundary is assigned a weight, which is a function of the congestion in the whole path of the net. The net with the highest weight is chosen first for rerouting. Since only improved paths are accepted in the process, the overall convergence is guaranteed. Figure 8 shows a balanced solution after rerouting.

The process can be visualized as the leveling of hilly terrain by pushing material from hill tops down the slopes. This results in lower and smoother contours with a small increase in total volume of material (net length).

PIN SELECTION

During the last stages of global wiring or the early stages of detailed wiring, it is advantageous to reassign nets to pins. The pins to which the nets must attach may often be permuted in small sets without any effect on logical function. For example, the input pins of a NAND or a NOR circuit are all equivalent. The exact choice of these pins has an effect on the number of channels which are available through a block, as illustrated in Figure 9. The objective of the pin selection analysis is to minimize the blockage of the wiring sources.

NET SEGMENTATION

After global wiring, the nets are assigned to certain horizontal wiring streets and vertical avenues for detailed wiring. Each street will contain a number of parallel segments which must be assigned to available channels. The wiring within each street or avenue is dependent on that in all the others. In particular, where a street crosses an avenue, the vertical and horizontal wiring are coupled. Still, this coupling is generally not strong enough to force the detailed wiring to use more channels than would be required for an uncoupled solution.

Figure 10 illustrates the segmentation of a net N, in the vertical direction. X_i's are the net points and a_i's represent the assignment points. After the vertical assignment process, net N is segmented into four independent subnets n_1, n_2, n_3, and n_4.

Figure 11 shows the horizontal segmentation of the same net N. It should be pointed out that only one segmentation is required for a wiring procedure.

CHANNEL ALLOCATION

The most constrained streets or avenues are wired first. The problem consists of a set of parallel segments to be assigned to channels. The constraints come from two sources. The first is that there may be fixed target points (pins) within the street or avenue. The second is that a segment which enters a street, from one side on a specific channel must be wired nearer that side than a segment which enters the street from the other side on exactly the same channel. Constraints of the second kind are called conflicts.
The algorithms used for channel allocation are repeated linear assignment of segments to channels using Munkre's method and an extension of the simple line pack procedures of Hashimoto and Stevens. The former is used when there are pins in the wiring street, the latter when the streets are clear. As mentioned earlier, some pin assignments can be deferred until the channel allocation phase.

An example of line packing in a horizontal street is given in Figures 12 through 15.

Net segments entering a street from above in the same channels used by other segments entering the street from below are in potential conflict. The net segment entering from above has to be assigned to a channel above the one assigned to the segment entering from below. This ordering
relation, (i.e., one segment is required to be wired above another) constrains the linepacking algorithm and, in some cases, leads to a set of constraints which are impossible to satisfy at all. Two such situations, the cyclic conflict and the chain, are illustrated in Figures 12 and 13.

It is clearly advantageous to remove these constraints, if possible, especially to cut all cycles and over-length chains. For this purpose, three straightforward methods are used. The first is to interchange logically equivalent pins of a logic block (e.g., two inputs of a NAND gate). The second is to introduce a short horizontal connection on the vertical plane which had the apparent result of moving the entry point of a segment into the street. The third is to wire a segment in more than one channel. By choosing an uncongested region of the street and dividing one horizontal segment into two segments with a vertical connector, it is possible to wire the two new segments in different channels and thereby satisfy previously impossible constraints. An example of such a solution is given in Figures 14 and 15.

The channel allocation program then scans the wire segments from left to right, filling one channel at a time. When one wire segment ends, the next nearest wire segment is selected to fill out the channel. This selection is conditioned by two considerations: the first is a conflict situation where a candidate segment is required to be above or below a segment which has not yet been wired. If the wiring of the candidate segment in the current channel precludes the wiring of the associated segment in the proper order, then the candidate segment is deferred. The second consideration is the affinity of the candidate segment to the side of the street in which the current channel lies. If two candidate segments are equally suitable from the point of view of linepacking, the one with the greater proportion of connections to that side will take precedence. Figure 16 illustrates the final results for the example shown in Figure 12. A "branch and
RESULTS

A version of this method was implemented in 1972 to wire bipolar chips. The results quoted in Reference 6 will be summarized here. A representative sample of 100 logic chips each containing an average of 125 logic gates and 136 nets. There were 10 vertical wiring avenues with eight channels each and 10 horizontal streets with four channels each. The programs ran in 325K bytes in an average of eight seconds CPU time on a 360/195. The wiring completion percentage in terms of segments, was better than 99 percent. The overall utilization of wiring space varied between 40 and 55 percent of the total length of metal which could be put on the chip.

The wiring programs exist within the framework of a larger physical design automation flow encompassing wirability analysis, partitioning, placement, interactive wire embedding and checking. In almost half the cases, the design is fully automatic (Figure 17). In the rest, the interactive wire embedding program permits a designer to finish the wiring in several hours.

In the years since 1972, thousands of chips have been wired this way. These automatic wiring programs have been a key element in the success of the automatic design system of which they are a part and the chip technology which they support.

REFERENCES