ABSTRACT

This paper outlines the basic data acquisition system as it might be configured for the home computing system. Allowance is made for data acquisition, interactive control with display, temporary data buffering, cassette storage of data, and computer control of external devices.

Cost/performance trade-offs are examined in each area where a variety of choices are available. For control, a simple keyboard and seven-segment display gives adequate results. Memory requirements are minimized by appropriate choices of data rates, operating system, and design of process control parameters.

The maximum cost savings are possible in the choice of A/D and D/A components, by careful decisions on converter speed and resolution, and on test design. The hobbyist has time/cash trade-offs options not available to industrial designers, thus hardware/software trade-offs can save either time or cash, depending upon which is most available to the hobbyist.

MEMORY CONSIDERATIONS

The available memory has been divided into Control Memory and Data Buffer. It is desirable, but not mandatory for all the Control Memory to be RAM. By means of cassette loading, it is simple to start up the system, and by keeping all programs in RAM it is possible to quickly modify the operating system for different tasks. The Data Buffer can be RAM, shift register or First-In-First-Out (FIFO) buffer, depending upon how the data is to be stored for later study. The total amount of system memory can be greatly minimized if the operating system allows individual data block storage on cassette as the data is received. The choice of RAM, shift register or FIFO will depend entirely upon the incoming data rate. For example, if the cassette system accepts data at 300 baud (30 characters per second), data rates faster than 300 baud require RAM storage. A steady data rate of 300 baud would allow direct storage on tape, with RAM only for temporary storage while each byte of data is formatted for transfer to tape. Perhaps 95 percent of all routine data acquisition applications will have a lower data rate, so that data can be received, formatted and stored in data blocks using a shift register. For example, a 1024-bit static shift register will store 128 8-bit characters; at 300 baud, it takes just over four seconds to dump the shift register onto tape. Between the extremes of 300 baud and 15 bytes per second, the FIFO can replace RAM as a data buffer. This is because the FIFO will accept and transfer data asynchronously at both input and output ports, so long as the average input rate does not exceed the output rate.
One special case also dictates the use of RAM for data storage: if the entire block of test data must be manipulated, analyzed or normalized in terms of the total test result, it is usually far more efficient to store the entire block of data in RAM rather than store it incrementally on tape. In the latter case, the tape might have to be played back a number of times before the calculations have been completed. The data storage can be minimized with data compression techniques; the total amount of RAM needed will still have to include workspace area for the data manipulation.

The previous data discussion was simplified by the implied assumption that data comes only in single-byte packets. This is rarely so; even if the output is from a single, 8-bit A/D converter, such isolated quantities are essentially meaningless. One example of the simplest case might be monitoring a single temperature. If temperature variation with time is to be recorded, the test can be arranged so that a measurement is taken every ten seconds. By recording the test starting time, the time of each sample can then be computed and need not be recorded. A much more common instrumentation problem requires recording of two or more variables from each test condition. One parameter will be the independent variable and all the others are dependent variables. (Dependent variables change as a result of changing the independent parameter.) One example: a single-tone test of an amplifier-speaker system. A tone is fed to the amplifier at varying levels (independent variable) and at each input level measurements are made of Total Harmonic Distortion (THD), temperature of the output transistors, and sound level from the speaker(s). This is a case where all three quantities would need to be measured and the computer might monitor THD or transistor temperature and vary input level accordingly. Thus, it depends upon the test whether the independent variable can be calculated (as in the time vs. temperature test above) or must be recorded. Careful test design can therefore minimize hardware, software and memory requirements.

It is now reasonably clear that the cassette operating system (software and hardware combined) should be such that start-stop operation of the tape is possible. The data would be output in a standard recording format such as the Kansas City Standard. The data in the tape output buffer should consist of sync characters (especially important for recording short blocks), ID characters, data characters, checksum characters (or other error detection scheme) and an ending character. As a result, the 128 characters stored in a 1024-bit shift register might represent only a few data points. If 8-bit A/D conversion gives insufficient accuracy, or if a BCD converter is chosen (a number of 3½ digit modules are available), data storage requirements will increase. In general, the UC will handle output from 10-bit, 12-bit and 3½ digit converters as two data bytes. Some tape routines store each byte as two ASCII characters, which could further limit the number of data points stored in the tape output buffer.

**DATA CONVERTERS AND THEIR INTERFACES**

Much of the cost of the data acquisition system can be in the data converters and their interface circuitry. Fortunately, there are a great number of low cost and medium cost monolithic and hybrid modules available; these have adequate accuracy and interesting combinations of features to make the choice difficult. A number of factors affect the decision process; required conversion speed, accuracy and resolution, microcomputer architecture, and location (remote or local). The two potentially most costly A/D parameters are conversion speed and accuracy/resolution, and the unit prices have fallen rapidly in recent months. Basically, the range of conversion speed is determined by the type of conversion—integration or successive approximation. Dual slope or multiple slope integrators with one to fifteen conversions/second and 8-bit resolution are quite inexpensive; moving to 500 conversions/second roughly doubles the price. Speeds beyond two milliseconds/conversion typically require successive approximation, and the speed jumps to roughly 20 microseconds/conversion. Faster conversion speeds are available but are a needless cost unless the microprocessor is much faster than the typical hobby machine. Increased accuracy and resolution jumps the price quickly, and typically slows the conversion at the same time. For example, one manufacturer’s price increased 30 percent and speed decreased by a factor of three in moving from 8-bit resolution (.4 percent accuracy) to 10-bit resolution (.1 percent accuracy), for the same type of conversion. The distinction between accuracy and resolution with regard to A/D converters is a topic beyond the scope of this paper. Some recent articles have made detailed explanations of A/D and D/A specifications.

The architecture of the microcomputer may exert some influence on the choice of A/D converter. If the converter will be expected to communicate directly with the data bus, the converter will need to have tri-state output lines or must be connected through tri-state buffers. On the other hand, many UC systems have programmable interface devices which allow direct communication with the converter. The
same interface device furnishes the address decode function, and some interfaces allow handshake and interrupt capability and can initiate the conversion process with a strobe line.

Figure 2 is a partial block diagram for a system with programmable interface circuits. Typically, these interface circuits reside in memory space (are addressed with memory instructions) and therefore pre-empt some memory addresses. Since virtually all hobby computers address at least 32 kilobytes of memory, this poses no problem for most data acquisition systems. Note that system components shown in Figure 1 will supplement the sub-system shown in Figure 2; Figure 2 merely illustrates how the programmable interface allows a much greater range of A/D component choices. This versatility usually allows lower priced converter components to be used.

If the data converters are remotely located, power must be furnished, control signals must go out and data must be returned. Since remote operation of the data bus is essentially impossible due to propagation delays, the send/receive circuitry which services the remote converter becomes a separate peripheral device. Consequently, the converter should be capable of autonomous operation on a single, low-power power supply and produce a serial data output. Reference 11 details systems which meet many of these requirements.

Because there is a bewildering array of different types of A/D converters which are normally reported, one type is often overlooked. This is the voltage-to-frequency converter (V/F), which has a number of advantages for the computer hobbyist.\textsuperscript{3,4} In particular, where conversion speed can be on the order of one second, 12-bit resolution (one part in 4096) is almost routine at very low cost, and 16-bit (one part in 65k) converters are available for about $50. This type of device is ideally suited for remote location in that its output is a pulse train whose frequency is directly proportional to the instantaneous input voltage or current. Its power requirement is relatively low and low power versions are available.\textsuperscript{8} At least one ultra-low power circuit using two standard IC's and a single power supply voltage has been reported.\textsuperscript{13} Finally, because the V/F is an integrating device, it tends to reject random noise, and has a wide dynamic range of operation.

To avoid a totally rosy picture, the V/F has two major disadvantages: slow speed and the data output stream. Because the output frequency is the parameter of interest, this signal must be counted. This is accomplished by having the uP gate the input to a counter (typically one second time intervals), and then reading the counter output lines as data (see Figure 3). A new problem now exists: resolution of even a garden-variety V/F module is 10 bits. To retain the full V/F resolution with an 8-bit uC, it is necessary to multiplex the counter output lines and read in two data bytes. However, IC counters which multiplex a number of digits into a bit-parallel, BCD word serial format are available. The BCD format is easily manipulated by most uC’s with software—decimal arithmetic instructions. If the full V/F resolution is not needed, set the time interval to avoid overflowing an 8-bit binary counter. Besides simplifying the interface, the data conversion time is reduced by the same ratio as the counter gate interval.

The fact that a V/F is a virtually perfect integrator simplifies measurements such as average quantity or total quantity, (for example, average temperature over a time interval or total energy used by a device). In the first case, a temperature related voltage serves as input to the V/F. A suitably scaled total count then represents the average temperature for the time interval of the count. In the second case, the V/F input must represent the power used by a device under test.

The final components in Figure 1 are the D/A converters and discrete control lines. The discrete control lines have been dealt with in a number of reports,\textsuperscript{15-17} but D/A converters have perhaps been slighted in home computing literature. Once again, the recent reports\textsuperscript{8-9} give a bewildering array of devices, but the spread of useful features is not so great. To be effective, D/A input data must be latched. Almost universally, low cost D/A modules do not have input latches, regardless of the device resolution. For this reason, the programmable interface (Figure 2) should be programmed as an output port to serve as data bus interface and data latch. Figure 4 shows low-cost alternatives. Figure 4A uses presettable counters (address decode and load strobe needed) to drive the D/A input lines, while 4B shows up/down counters serving the same need. Note the different output patterns (Figure 4C): the presettable counter (quad or hex latches are also suitable) gives a step-function output and the up/down counter version ramps to the final output. D/A converters have two serious faults—glitches and overshoot. A detailed treatment of these problems (cause and cure) is available,\textsuperscript{18} but in simplified terms, glitches are the result of unbalanced propagation times in the digital logic circuits and overshoot results from incomplete compensation of the analog output of the converter.
CONCLUSION

In summary, this paper has dealt with a complete, custom instrumentation concept for the home computing system, as represented in Figure 1. The intent has been to guide the designer toward cost-cutting decisions in microcomputer architecture, but with emphasis on low cost hardware. Obviously, if the desired system is to be less comprehensive, the cost drops immediately. It is also possible to trade software for hardware to effect cost savings. Reference 14 gives a number of ideas on hardware/software tradeoffs, but speaks from the standpoint of the cost-effective industrial designer. The home computer, when approached from the hobby standpoint, will have a different economic justification (usually to combine fun and accomplishment in a technical area, at an affordable cost). In other words, the hobbyist may always have to use his personal time instead of cash to accomplish particular goals. His computer may have a 5 uSec cycle time instead of 250 nSec (he can afford to wait), and if he enjoys software, hundreds of hours of program coding and de-bug to save $50 cash is an excellent investment. For the hardware hacker, adapting a published circuit or idea to work with junk-box parts is an exercise in frugality which also pays off handsomely in exercise of creative talent.

One example of software replacing hardware: let's update Figure 3 to Figure 5. The 10-bit V/F operates at 10 kHz; simply monitor the V/F output with a single input line and use a software loop to increment a totalizing register and a timer. Read the total counts at the end of the time interval, and Figure 3 becomes Figure 5. If the computer has a programmable timer, the input port of Figure 5 can be an interrupt line. If the timer can also set an interrupt, the computer has considerable time to mind other tasks while measuring a digital quantity. The program uses the V/F interrupt to increment a counter register until the timer times out. In this case, the faster computers will give better absolute accuracy because interrupt service is faster.

REFERENCES

7. "Designers are Looking Closely at New Monolithic DACs and ADCs," Electronic Design, 13, June 21, 1976, p. 28.