Prospective capabilities in hardware*

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ABSTRACT

Today we can look back over the past thirty years and view the entire history of the electronic digital computer! In addressing the topic of prospective capabilities in hardware, this paper first attempts to extrapolate, from today's state-of-the-art and vantage point, general industry-wide trends and likely achievements. Then, an effort is made to cover in more detail specific areas of interest to the ERDA community. Subjects discussed include available large-scale computers—their architecture and viability. The microprocessor's impact on computer systems is considered, and potential applications of the microcomputer are identified. Then mass storage offerings and their role in predicted memory hierarchies is assessed; progress in the development of alternate storage technologies is reviewed. New products and anticipated innovations in peripheral and input-output equipment, probably the most lethargic segment of the dynamic hardware market, are described, and a survey of network and communications activity examines future directions this rapidly-expanding field might be expected to follow.

Whenever possible in each of these areas, examples with descriptive characteristics, accompanied by cost and performance statistics, are presented in support of the initially-forecast broad technological trends. These examples, chosen for illustration, represent new hardware products, advanced technologies in the developmental stages, or planned enhancements of existing product lines.


INTRODUCTION

Beginning in 1946 with the dedication of the ENIAC at the Moore School in Philadelphia, this history is generally perceived as a sequence of eras. These eras, traditionally referred to as generations, are characterized by the technology employed by the computer industry during that period. The history of the computer industry, as customarily represented, is shown below with the fourth generation introduced to reflect the technological advances of this decade.

The transition from the first to second generation is clear-cut, defined by the industry's shift from vacuum tube to transistor technology. Emergence of later generations becomes blurred as the increased investment in the existing technology, coupled with the need for acceptance on a cost-performance basis, serves to retard the new alternative technologies. For example, the incorporation of large semiconductor memories was postponed by economic considerations until production quantities reached proportions permitting the technology to compete with the entrenched magnetic core storage.

In addressing the topic of prospective capabilities in hardware, this paper first attempts to extrapolate, from today's state-of-the-art and vantage point, general industry-wide trends and likely achievements. Then, an effort is made to cover in more detail specific areas of interest to the ERDA community and the agency's environmental science and analysis programs. Subjects discussed include available large-scale computers—their architecture and viability. The microprocessor's impact on computer systems is considered,
and potential applications of the microcomputer are identified. Then, the recently-announced mass storage offerings and their role in predicted memory hierarchies is assessed; progress in the development of alternate storage technologies is reviewed. New products and anticipated innovations in peripheral and input-output equipment, probably the most lethargic segment of the dynamic hardware market, are described, and a survey of network and communications activity examines future directions this rapidly-expanding field might be expected to follow.

Whenever possible in each of these areas, examples with descriptive characteristics, accompanied by cost and performance statistics, are presented in support of the initially-forecast broad technological trends. These examples, chosen for illustration, represent new hardware products, advanced technologies in the developmental stages, or planned enhancements of existing product lines.

TECHNOLOGICAL TRENDS

In 1970 the largest second-order suppliers to the computer industry, the semiconductor manufacturers, were doing a 348 million-dollar business annually, producing logic components and peripheral system elements while developing the technology to permit integration of larger logical functions on a single semiconductor chip.1 Large-scale integration, the hallmark of the fourth generation, is the name given the technology used to produce high-density electronic circuits. Although not defined precisely, it is generally interpreted to imply over a hundred "gates", or individual circuit functions, at a density exceeding 50,000 components per square inch.2

Major benefits and industry-wide trends resulting directly from the steady improvement in production of LSI modules and fabrication techniques are:

- reduced cost per logic function, or memory bit, with an accompanying decrease in physical size,
- increased complexity with implied enhanced capability and performance, and
- improved reliability.

These trends can be expected to continue. Today, chips less than a quarter of an inch on an edge incorporate well over 20,000 components at a cost under a small fraction of a cent per component.3 This low cost is achieved primarily by economies of volume production, although advances in semiconductor fabrication techniques, and adoption of computer-aided design (CAD), manufacturing (CAM), and automated component testing procedures have played a part. The reduction in the number of interconnections and components brought about by LSI has contributed to the realization of both increased complexity and higher reliability in the hardware product. It is, and will remain, expensive to produce custom-tailored LSI; standardized circuitry is required for low prices. A plot showing the density and cost of integrated-circuit components over the 1960-1980 time period reconstructed from an August 1973 Scientific American article is shown as Figure 2.4

Semiconductor manufacturers concentrated much of their early LSI effort on the production of computer memory arrays because of their inherent regular structure and potential volume market as a replacement for magnetic-core storage. Fabrication technology known as MOS, for metal-oxide-semiconductor, was introduced to achieve higher-component density than realizable with the older, higher-speed "bipolar" technique. Early utilization of semiconductor memories was limited, because of cost considerations, to read-only memory (ROM) control storage or to small arrays of read/write memory (RAM) employed, in hierarchical memory organizations, as buffers or caches. In 1971 IBM delivered the first System 370/145 with its semiconductor main memory, and finally, during the 1972-73 time-period, semiconductor storage overcame the cost advantage maintained for so long by magnetic-core technology.

The MOS process was also utilized in the manufacture of chips for the popular, electronic desk and pocket calculators, which created a new large-volume semiconductor market. As an outgrowth of this effort, and in an attempt to stimulate sales of its semiconductor memory modules, Intel Corporation in 1971 announced the first, programmable, single-chip LSI processor. Soon other microprocessors appeared; these "micro" versions of the traditional CPU—the computer's control and arithmetic-and-logic units—were quickly incorporated in a variety of applications ranging from electronic games to point-of-sale and bank terminals, and laboratory instrumentation. Combined

![Figure 2—Density and cost of integrated circuits for the period 1960-1980](image-url)
with timing, memory, and input-output facilities the long-heralded "computer-on-a-chip", or perhaps a few chips, had arrived. The microcomputer is here, and in time we can expect a nanoprocessor, capable of instruction times in the range of 100 nanoseconds. Nano-processors can be implemented in bipolar technology if kept simple; bipolar has yielded speeds well under 100 nanoseconds for 1024-bit RAM and ROM chips, and cost is decreasing rapidly to levels comparable to the MOS devices. A silicon-on-sapphire (SOS) approach offering increased speed and component density shows promise for the future.

Entire new areas of applications have become accessible to the computer industry with the advent of the inexpensive yet powerful microprocessor. Trends in progress, or anticipated, as a result include:1,6,7

- "intelligence" added to practically every type of control and data entry equipment (i.e. remote sensor and monitoring devices, automobiles, appliances, process control, data entry, graphics, and word-processing terminals),
- dedicated small digital systems incorporated in computer subsystems (e.g. computer peripherals controllers, communications controllers), and
- evolutionary changes in system design occasioned by the availability of near "zero" cost hardware and the attendant distributed intelligence possibilities.

In addition to the trends forecast as directly attributable to LSI technology and the availability of microprocessors, a review of characteristics, components, and the organization postulated for next decade's computer indicates:6,9

- processor speeds greater than 100 MIPS (million instructions per second),
- increased size (up to 100 megabytes) of semiconductor main memory,
- available on-line archival mass storage facilities using different technologies,
- architecture directed toward multiprocessor network configurations utilizing multilevel memory, and computer, hierarchical organizations,
- extensive use of microcode to accommodate dedicated or special processes and distributed-function concepts,
- decentralization of communications, input-output, and peripheral file management subsystems,
- firmware implementation of many of today's operating system features and other system software,
- incorporated performance-measurement monitoring, maintenance, and error-logging, and fail-soft and fault-tolerant design for increased hardware reliability and availability.

Historically, computers have been classified as small, medium, or large-scale primarily on the basis of price and performance. Size defined the minicomputer of the sixties and the microcomputer in this decade. Such distinctions are no longer relevant; a full spectrum of computer power from microprocessor to mainframe is available for the choosing. The user pays his money and takes his choice, and he has progressively, year by year, been offered more performance for his dollar. This trend can be expected to continue, particularly at the low end of the spectrum. Tomorrow's moderately-priced computer system will afford the user much the same computing power as today's high-priced spread; the low-priced system can be expected to provide moderate capability at a reduced price, etc. Price in the computer industry is negatively correlated with quantity, or market volume. This coupling could cause the most significant impact on the scientific community, and ERDA, of all these trends. The larger, more powerful, state-of-the-art processors required for ERDA's programs will tend to represent an increasingly smaller fraction of the market; consequently, fewer such computers will be developed, and those will tend to be expensive when compared, on a cost-performance basis, to the models produced in response to market demand. Two possible reactions, should such a situation come to pass, are the approach taken by the Controlled Thermonuclear Research (CTR) Division in providing computer capability for its program, and the action taken earlier by the AEC in ensuring adequate computational resources to meet laboratory requirements. The CTR approach is to provide the top-of-the-line, number-crunching capability at a single-site, the Lawrence Livermore Laboratory, together with the network and station facilities necessary to make this power accessible to off-site program participants. The LARC and STRETCH projects were cooperative ventures undertaken by the AEC with Remington Rand and IBM to develop the computer capability needed for the Commission's research and development activities.

LARGE-SCALE COMPUTERS

About four years ago at the Idaho Falls topical meeting of the American Nuclear Society's Mathematics and Computation Division, Jack Worlton of the Los Alamos laboratory, presented an entertaining talk on a theme similar to the one covered by this paper. At that time, he noted that the IBM 360/195 and the CDC 7600, both capable of executing ten million instructions per second, were the fastest computers installed, and speculated that even faster computers would be delivered in the next few years.10

The number of faster computers delivered in the intervening years has been dismally small, and their power has not been uniformly impressive. ILLIAC IV, the Texas Instruments ASC (Advanced Scientific Computer), and the Control Data Corporation's STAR-100, all unconventional machines from a system architect's point of view, have arrived on the scene, each culmi-
nating about ten years of research and development effort. Standing in the wings is CRAY-1, the initial product of Seymour Cray's Cray Research, Inc., which is expected to provide five times the performance of the CDC 7600 when delivered in January of next year.

Meanwhile, work on the CDC 8600 expected as a follow-on to the CDC 7600 has been discontinued; neither the postulated IBM 370/178 nor FS, the giant's Future System has emerged. Instead, CDC is upgrading their 7600 system, IBM has announced enhancements to their 370/158 and 168, UNIVAC has souped-up its 1100 series, and Amdahl recently delivered its first machine, the 470 V/6 aimed at the IBM 370/168 marketplace. The future of large-scale, fast and powerful scientific computers is unclear.

ILLIAC IV is generally described as a parallel computer, or array processor. The concept was first explored in the early sixties at the Westinghouse Electric Corporation on the premise that large-scale computing could be characterized as repetitive execution of the same algorithm on different data streams. The assumption that much of the cost of that day's conventional computer was associated with the control logic also had an influence on the design. Inherent in the Westinghouse SOLOMON design is the concept of many simple, identical processors, each programmed by a common central control unit to directly simulate the physical process being studied. The basic system considered, consisted of multiple processing elements, (PEs), configured in an array, with each PE a complete arithmetic-and-logic unit capable of executing a full instruction set. Each element contained its own memory unit, could optionally execute or ignore a given instruction, and could transfer data to any of its four nearest-neighbors.

During the latter part of 1966 a project was initiated at the University of Illinois, funded by the Advanced Research Projects Agency (ARPA), providing for construction by the Burroughs Corporation of the ILLIAC IV parallel computer based on the prototype SOLOMON studies. Sixty-four PEs were implemented in ILLIAC IV, each with a memory unit capable of storing 2048 64-bit data entities in a variety of 8-, 32-, or 64-bit fixed and floating-point formats. In addition to this 8.4 million bits of main memory, the machine has a one-billion-bit diskfile secondary memory, and a one-trillion-bit archival storage subsystem. A front-end Burroughs 6500 computer was incorporated in the design to control the laser-beam read and record third-level memory, the usual array of peripheral card, printer, tape, disk and display equipment, and telephone-line communications. The machine was designed to be accessible to ARPA research contractors via the ARPANET resource-sharing network. Since the ILLIAC IV project was moved to the NASA Ames installation in California little has been heard of it, except for occasional mention of the fact that the system is not operational. At the IEEE Lake Arrowhead Workshop in 1973 D. L. Slotnick, who was responsible for the project at the University of Illinois, was quoted as commenting that in an up-to-date miniaturized ILLIAC IV the processing elements would be in the reading heads of a disk.

Starting with the overlapping of input-output and peripheral device operation with CPU execution 15 years ago, designers have successively introduced forms of parallelism in the initially serial stored-program computer in an attempt to achieve higher-performance with existing components and state-of-the-art technology. Pipelining techniques are implemented which segment the various stages of instruction execution and pass operands from one to the next to allow many operations to be in progress simultaneously. Multiple functional units are incorporated to permit several operations to be executed simultaneously, and microprogram control is utilized to meet the associated timing constraints. To provide the supply of operands required at a rate consonant with the CPU operation memory modules are interleaved, data paths widened, instruction stacks with "look ahead" logic and cache memories are added. In three of the available large-scale systems—the CDC STAR-100, TI's ASC, and the CRAY-1—vector capabilities have been included in the machines' instruction sets to achieve increased processor speed, leading these computers to be referred to as vector processors.

Development programs for the STAR-100 and ASC were initiated in the mid-sixties and, to date, two STARs and six ASCs have been delivered. Both STAR-100s are at the Lawrence Livermore Laboratory where personnel have been involved in the STAR development from its inception. Three ASCs are in use at Texas Instruments, one for system development and two on contract seismic applications; a fourth is employed on seismic work in the TI Amstelveen, Holland facility, and the fifth and sixth are at the Army Ballistic Missile Defense Agency Huntsville research center and the NOAA Geophysical Fluid Dynamics Laboratory at Princeton University. When Cray Research, Inc. was established in April of 1972 work began on the initial CRAY-1 machine. It is expected to be available for delivery in January 1976, and a second unit is under construction in Chippewa Falls.

A table summarizing characteristics of these three machines is shown as Table I.

Several features of these machines deserve mention as illustrative of the trends projected earlier. In the STAR-100 the CPU's stream unit, which directs the instruction and operand streams into the arithmetic unit, uses microcode resident in two 80-nanosecond ROM components to initiate and terminate vector and string operations and to monitor interrupt conditions. When an interrupt occurs, information necessary to restart is saved, an interrupt flag is set, and the microcode program triggers the exchange from job to monitor mode. In the stream unit, too, is the 256 64-bit

From the collection of the Computer History Museum (www.computerhistory.org)
TABLE I—Characteristics of the Available Vector Processors

<table>
<thead>
<tr>
<th></th>
<th>CPU</th>
<th>STAR</th>
<th>ASC</th>
<th>CRAY-1</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>CPU:</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Instruction size</td>
<td>32</td>
<td>32</td>
<td>16</td>
<td>16 or 32</td>
</tr>
<tr>
<td>(bits)</td>
<td>64</td>
<td></td>
<td>32</td>
<td></td>
</tr>
<tr>
<td>Clock period</td>
<td>40</td>
<td>60</td>
<td>12.5</td>
<td></td>
</tr>
<tr>
<td>(nsec)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Instruction stack/buffers</td>
<td>32 words (2048 bits)</td>
<td>16 or 32 words (512 or 1024 bits)</td>
<td>256 parcels (4096 bits)</td>
<td></td>
</tr>
<tr>
<td><strong>Functional units</strong></td>
<td>3</td>
<td>1, 2 or 4 pipes, with memory</td>
<td>12 integer add</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 string unit</td>
<td>buffer unit &amp; arithmetic unit</td>
<td>1 integer multiply</td>
<td></td>
</tr>
<tr>
<td></td>
<td>2 floating-point units</td>
<td>unit</td>
<td>2 shift</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 pop. count</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2 logical</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 floating add</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 floating multiply</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 reciprocal approx.</td>
<td></td>
</tr>
<tr>
<td><strong>MEMORY:</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Technology</td>
<td>magnetic core</td>
<td>bipolar semiconductor</td>
<td>bipolar semiconductor</td>
<td></td>
</tr>
<tr>
<td>Word length (bits)</td>
<td>64</td>
<td>32</td>
<td>64</td>
<td></td>
</tr>
<tr>
<td>Address space (words)</td>
<td>4 \times 10^12</td>
<td>16M</td>
<td>4M</td>
<td></td>
</tr>
<tr>
<td>Data path width (bits)</td>
<td>512 (= 1 s (uper) word)</td>
<td>256 (= 1 octet)</td>
<td>64</td>
<td></td>
</tr>
<tr>
<td>Cycle time</td>
<td>1.28 \mu s</td>
<td>160 nsec</td>
<td>50 nsec</td>
<td></td>
</tr>
<tr>
<td>Size (words)</td>
<td>512K or 1M</td>
<td>128K to 16M*</td>
<td>1M</td>
<td></td>
</tr>
<tr>
<td>Organization/interleave</td>
<td>32 banks</td>
<td>8 module</td>
<td>16 banks</td>
<td></td>
</tr>
<tr>
<td>Maximum band width (bits/sec)</td>
<td>200 \times 10^6</td>
<td>400 \times 10^6</td>
<td>80 \times 10^6</td>
<td></td>
</tr>
<tr>
<td>Maximum band width (bits/sec)</td>
<td>12.8 \times 10^9</td>
<td>5.1 \times 10^9</td>
<td>1 parity bit/word</td>
<td></td>
</tr>
<tr>
<td>Error checking</td>
<td>2 parity bits/word</td>
<td>single-bit error correction</td>
<td>double-bit error detection</td>
<td></td>
</tr>
<tr>
<td><strong>LOGIC:</strong></td>
<td>TCS</td>
<td>TCS</td>
<td>TCS</td>
<td>TCS</td>
</tr>
</tbody>
</table>

* optional MOS semiconductor memory extension of up to 1M words with 1 \mu s cycle time and 64 \times 10^6 band width

** TCS (transistor current switch), ECL (emitter-coupled logic)

From the collection of the Computer History Museum (www.computerhistory.org)
memory chassis positioned four on each side of the CPU in the CRAY-1 main frame.

Contained in the central processor are four instruction parcel buffers (IPBs), over 150 program-addressable registers, and 12 independent algorithm or functional units. Each CRAY-1 instruction is either a one-parcel (16-bit) or two-parcel (32-bit) instruction. The 64-parcel instruction buffers are organized in 4 to 1 correspondence with the 16-memory banks so that the first four parcel positions in a buffer are always filled from bank 0, parcels 5 through 8 come from bank 1, etc. This feature, combined with the use of four 64-bit paths, in parallel, between memory and the IPBs, makes possible a transfer rate of four words per clock period. Buffers are filled in turn; whenever an instruction fetch from memory is required, the “least recently filled” IPB is used. The fetched instruction is always read in with the first parcels regardless of its memory bank source and associated buffer-position destination.

The machine complement of program-addressable registers resembles a greatly-expanded CDC 7600 collection. Registers have been added to hold vector instruction parameters and to serve as source and destination addresses for operands in, up to 64-element, vector arithmetic and logical instructions. In addition, the eight principal address-length registers used as address registers for memory reference and index registers, and the eight principal word-length registers which act as source and destination registers for scalar operands, are each backed-up by 64 secondary registers designed to provide quick-access, temporary storage. Operands can be recalled from secondary to principal register storage in one clock period, and the secondary registers can be loaded from memory, or stored away in stream-fashion with a single block copy command at the rate of one clock period per operand after a startup period. Contents of a vector register are stored in, or loaded from, memory by specifying the initial address, an increment for succeeding addresses, and the vector length, at a one-clock-period rate once eight elements have been transferred.

Functional units are designed with one-clock period segmentation; the source and destination addresses are limited, and the algorithm chosen so that the time required for each unit to complete its task is fixed. In vector mode results are produced at a one-clock-period rate, and these results may interact with other vector instructions in “chained” operations since all functional units have the same result rate. Three integer add units, an integer multiply, two shift units, a population counter, two logical operations units, and floating-point add, multiply, and reciprocal approximation units are included in the central processor. The machine performs floating-point division by reciprocal approximation; four instructions are necessary to obtain 48-bit precision. When vectors longer than 64 elements are used, programming is required to divide them into 64-element sequences for processing.

Twelve full-duplex, 64-bit wide, input-output channels are included in the CRAY-1 system; however, the only peripheral equipment supplied will be the CDC 819 disk which is used as the resident device for the operating system. The system described is priced at 7 to 8 million dollars and purchasers are expected to acquire their unit record, disk, tape, display, and terminal equipment from other vendors.

Today, although both STAR and ASC systems are in operation it is difficult to find performance comparisons with conventional machines or published benchmark problem results. The “promised” computing power of vector processors a decade ago has yet to be realized. The architecture is designed to optimize vector-mode operations in which the vector elements are at contiguous storage locations, and the number of elements in the vector is large; the latter is especially true in the STAR-100 implementation. Consequently, it is essential that programs written for these vector processors exhibit a high ratio of vector to non-vector (scalar, branch, test, execute) instructions and that both code and data be ordered to minimize memory references and maximize parallel operations. Over the past six years LLL computer personnel have been working on the construction of the STAR operating system and related software to achieve their announced goal of incorporating the machines as worker computers in the Laboratory’s OCTOPUS time-sharing network. During this same period they have developed techniques and methods for transforming existing large production codes into “vectorized” STAR code. This has proved to be an arduous task.

Texas Instruments has, since 1968, been developing a sophisticated FORTRAN compiler, ASC NX, with array-oriented language extensions to generate “vectorized” code for their machine. The NX compiler translates FORTRAN DO-loops into vector instructions, and, if instructed that the code is for a multi-pipe machine, can introduce parallel instruction streams. An extensive optimization analysis is performed and as output, the programmer receives information intended to assist hand-tailoring of the source code to allow further iterative compiler optimization, if desired. Factors to be considered, and techniques, for improving the efficiency of execution of ASC scalar instructions were presented in a recent paper.

Table II summarizes performance statistics which have been reported for the two machines.

The CRAY-1 second generation vector processor is obviously intended to take care of many of the problems that have been encountered in attempting to use the first-generation processors, and both CDC and TI are planning for the future. CDC expects to replace their core memory with a bipolar semiconductor memory and to add a front-end computer to the system. Before the year is out, they intend to announce STAR as a product, send staff to Livermore to assist with the STAR-OCTOPUS merger, deliver model 108 to
NASA Langley, and add 104 to their own CYBERNET computer service network. TI is readying a 61,500 word per second mass-storage videotape subsystem for use with the serial 4 ASC at the Princeton Geophysical Fluid Dynamics Laboratory, and that machine's main memory will probably be expanded to 4M words utilizing a 1024-bit memory chip with a 100 nsec store time instead of the present 256-bit chip. Serial 7 will be delivered to the Naval Research Laboratory in January of next year and late in 1976 announcement of a 6-megaword compatible channel can be expected. Presently being looked at as a cost reduction measure is a 16M-word-memory design incorporating a 4K MOS chip with 200 nsec access and increased interleaving. The company is interested, also, in locating a customer seeking faster scalar capability; they believe a two- to fourfold increase in speed can be realized within two years, following such an order.

While the array and vector processors were being designed and constructed, the mainstream large-scale computer systems were evolving toward a flexible, modular architecture in which the major system components such as memory, processor, and input-output control are treated as logically separate entities. Keenly aware of the user's evergrowing investment in applications programs and computer-based data, manufacturers have attempted to structure their product lines to accommodate the user. The number and performance capabilities of the component units can be tailored to meet budget constraints and growth requirements, and technological advances offering improved component performance can be incorporated quickly and effectively, all with minimal impact on the user's operation. Increasing emphasis is being placed on system reliability and availability.

Control Data Corporation's 7600 has found wide acceptance in ERDA laboratories and the nuclear industry where 18 of the 38 delivered systems are employed. Later this year the company plans to enhance this system with expanded and improved memory components. Characteristics of the current and proposed 7600 SCM and LCM units appear in Table III. The CTR Computer Center at Livermore is scheduled to receive the first of the small semiconductor memory models during the latter half of this year, and the revamped 7600 can be expected to appear in CDC's product line about a year later.

IBM announced the 168-3, an enhancement of their 370 Model 168, in March of this year; first customer shipment is scheduled for June. Using a new 1K bipolar chip IBM has increased the machine's 80 ns cache buffer memory capacity from 16K to 32K bytes. New microcode in the processor's reloadable control increases the speed of a number of frequently-used instructions and internal interrupts. A service processor added to the 168-3 monitors and stores machine status information to aid engineers in servicing and diagnosis of machine failure; the service processor also provides a teleprocessing interface with the company's Field Engineering Large Systems Support Center. A 5 to 13 percent increase in performance has been predicted for the improved 168, which is priced at 5 million dollars when equipped with the top-of-the-line 8-megabyte memory.

### Table III—Characteristics of CDC 7600 Memories

<table>
<thead>
<tr>
<th>Technology</th>
<th>CURRENT</th>
<th>PROPOSED</th>
</tr>
</thead>
<tbody>
<tr>
<td>Size (words)</td>
<td>32K or 64K</td>
<td>64K or 128K</td>
</tr>
<tr>
<td>Organization (banks)</td>
<td>16 or 32</td>
<td>16 or 32</td>
</tr>
<tr>
<td>Cycle time (nsec)</td>
<td>275</td>
<td>1700</td>
</tr>
<tr>
<td>Holding register (words)</td>
<td>8</td>
<td>16</td>
</tr>
<tr>
<td>Error checking</td>
<td>5 parity bits/word</td>
<td>single-bit error correction</td>
</tr>
</tbody>
</table>

### Table II—Performance Statistics and Comparisons of Vector Processors Relative to the CDC 7600 and IBM Model 195

<table>
<thead>
<tr>
<th>COMPUTATIONAL PROBLEM</th>
<th>CDC 7600</th>
<th>OR IBM 360/195</th>
<th>IBM ASC</th>
<th>CRAY-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Scalar</td>
<td>1</td>
<td>0.25</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>Vector</td>
<td>(10 elements)</td>
<td>1</td>
<td>0.4</td>
<td>6</td>
</tr>
<tr>
<td></td>
<td>(25 elements)</td>
<td>1</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(300 elements)</td>
<td>1</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(1000 elements)</td>
<td>1</td>
<td>5</td>
<td>10</td>
</tr>
<tr>
<td>Scatter-Gather</td>
<td>1</td>
<td>0.67</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>1-D HYDRO</td>
<td>1</td>
<td>1.6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Matrix Inversion</td>
<td>(25×25)</td>
<td>1</td>
<td>1.58</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(50×50)</td>
<td>1</td>
<td>1.75</td>
<td></td>
</tr>
<tr>
<td>Matrix Multiplication</td>
<td>(25×25)</td>
<td>1</td>
<td>1.27</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(50×50)</td>
<td>1</td>
<td>1.32</td>
<td></td>
</tr>
<tr>
<td>GFDL models</td>
<td>1</td>
<td>3 to 14</td>
<td></td>
<td></td>
</tr>
<tr>
<td>GFDL jobstream</td>
<td>1</td>
<td>2.5 to 3</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
In March, too, Sperry Univac announced its 1100/40 system, successor to the 1100 as the largest of the firm’s large-scale systems. The 1100/40, like the 1110, has two levels of memory: a primary memory with from 28K to 512K 36-bit words and an extended memory with 128K to 1M-word capacity. Implemented in 1K bipolar the 1100/40 main memory offers double the primary storage available with the earlier plated-wire technology. This memory has 280 ns read and 380 ns write time, while the extended MOS memory for the 1100/40 has an 800 ns cycle time. The processor component in the system is the Command/Arithmetic Unit (CAU) with 300-nanosecond basic instruction time and 1.8 MIPS capability. Input/Output Access Units (IOAUs) control communications among system components and peripheral input-output. Multiprocessor configurations as announced offer up to four each CAUs and IOAUs. Gains of 10 to 25 percent in throughput over the 1110 are expected for the new system. Recently, NASA selected this system for a potential 8-million-dollar space shuttle simulation complex at the Houston Johnson Spacecraft Center. The NASA system will have 6 CAUs and 3 IOAUs extending the 1100/40s multiprocessor capability.

Advanced LSI technology is stressed in the newest entry in the large-scale computer industry, the Amdahl 470 V/6. This machine is designed to compete for the IBM 370/168 market using slightly-modified IBM software systems and, like the CRAY—1—letting the customer select his peripherals from other vendors. Central processor circuits are custom-designed emitter-coupled logic. The Amdahl LSI chips, 10 mils thick and measuring 0.154 inch square, can hold up to 100 circuits; speeds on the chip are on the order of 600 picoseconds. Chips are mounted on a ten-layer multilayer board in specially-designed multichip carriers, (MCCs), which serve as the field-replaceable unit. Fifty-one MCCs, each containing about 3000 circuits, make up the 470 V/6 CPU and channel. From 1 to 8 megabytes of directly-addressable MOS memory is offered with a 18K high-speed bipolar cache and 16 I/O channels in the basic configuration. The channels provide standard 360/370 interfaces for attachment of peripheral devices. At the system console, equipped with keyboard/CRT display, minicomputer, cassette tape reader, modem, and disk storage unit, console operation, hardware control, and system maintenance functions are carried out. The first Amdahl computer, delivered to NASA’s Institute for Space Studies at Columbia University the beginning of June, was up and running in a week’s time. Table IV shows some reported single-job NOAA benchmark comparisons of the 470 V/6 with the IBM Model 195.

### MICROPROCESSORS AND MICROCOMPUTER APPLICATIONS

In fiscal year 1974 over half of the computers in the Atomic Energy Commission were Digital Equipment Corporation machines. A large majority of these were minicomputers incorporated in dedicated laboratory applications. It is reasonable to expect that, in the future, with the growing availability of microprocessors and microcomputers, the instrumentation and computer requirements for many ERDA laboratory applications will be supplied by cheaper, smaller, more specialized, and more reliable LSI technology. This year DEC introduced an LSI-11 microcomputer at the low end of its PDP-11 product line. An LSI-11 configured with 64K bits of read/write memory, 64K bits of PROM (programmable ROM) memory, a 16-bit parallel input-output interface, and floating-point arithmetic is available at a cost of around 1500 dollars. The PDP 11/40 instruction set is emulated in microcode.

Two laboratory applications of microcomputers at LLL were reported in a paper presented at a February computer conference. One dealt with tritium monitoring in various environments; the second was concerned with calculations on spectral data output from a pulse height analyzer. LSI technology is particularly adaptable to the area of environmental monitoring, and the low cost of microprocessors and microcomputers can be expected to lead to new applications not previously considered.

### MASS STORAGE SYSTEMS

In the past year with the announcements of the IBM and CDC mass storage systems there has been a resurgence of interest in archival mass storage to replace manually-mounted magnetic tape, to allow installations to service evergrowing numbers of interactive users, and to place burgeoning data bases on-line particularly in a multi-computer environment. To appeal, such systems must be available at a cost approximating that of magnetic tape and be easily integrated into the customer’s operation.

The IBM 3850 Mass Storage System (MSS) is a hierarchical storage system capable of storing and managing up to 472 billion bytes of data on-line. The data is stored on 64-foot lengths of magnetic tape, about 3 inches wide, “spooled” in plastic cartridges, 4 inches wide and 2 inches in diameter. Data re-
corded on the tape as IBM 3336-1 cylinder images, each cylinder appearing at a fixed location on the tape. A single cartridge can contain 202 cylinders; a pair of cartridges, the equivalent of one disk pack, is referred to as a mass storage volume (MSV). All space in the MSS is managed in terms of these MSVs. Cartridges are stored in cells in a honeycomb arrangement in the unit. Data are transferred from the cartridges to staging buffers (dedicated 3350 drives) when requested. Once staged there, data are accessible just as any other data resident on a 3330. When no longer needed, and the space on the staging device is required for other data, any "cylinder" containing new or updated data is destaged back onto the data cartridge. MSS uses a "least recently used" replacement algorithm. Important concepts in the IBM 3850 implementation are the ideas of virtual device and virtual volume. The virtual device concept allows more drives to be addressed than actually exist in the hardware configuration. The virtual volume concept allows many partial MSVs to reside on a single staging drive, or different parts of an MSV to reside on several staging drives. Industry sources believe IBM already has 700 to 1000 firm orders for the 3850.37

The CDC system is composed of a mass storage adapter (MSA) unit and a mass storage facility (MSF) with two, three, or four read/write stations mechanically coupled to a cartridge storage unit.32 The cartridge file provides storage for up to 16 billion characters. The MSF may be configured modularly in sizes greater than 16 billion bytes. A single MSA can handle up to 8 or 16 elements depending on the model; an element is defined as either a read/write station or a cartridge storage unit. Up to 8 MSAs can be attached to a single 3830-2 controller. Data in the MSF are recorded on 100-inch lengths of 2.7-inch-wide magnetic tape in a 9-track format at 6250 bpi density. One hundred and forty-four tracks can be recorded. The tape strip, containing up to 8 megabytes of information, is enclosed in a plastic cartridge, measuring 1.125" x 1.25" x 3.3". Two thousand such cartridges are stored in the rectangular array of cells making up the cartridge file. When a data set is required by the applicable data set cartridge is located by its x-y coordinate address in the file, selected from its cell by the unit's cartridge selector, a pneumatic pick mechanism, and transported to a read/write station. At the station the cartridge is opened, the tape unwound, and drawn into two vacuum columns for reading. After being read the tape is rewound into the cartridge, and the cartridge is sealed and returned to its file location. The tape is never detached from its protective housing. Data can be staged to any available disk space in the host system, or staging can be eliminated altogether. Data sets can be read directly to main memory and returned directly to the cartridges, if desired. Two cartridge I/O drawers, with 8 cartridge slots apiece, allow the operator to enter and remove cartridges from the unit manually, and a write-inhibit plug can be used to ensure that master library tapes are not written over accidentally. A CDC MP16 minicomputer incorporated in the MSA performs on-the-fly error correction and detects illegal commands and incorrect sequences. Control Data estimates ten million dollars has been spent over the past five years developing this system.39 One of the first systems scheduled for shipment in the fourth quarter of 1976 will go to LLL.

Two other currently-available mass storage systems are the CalComp Automated Tape Library (ATL) and the Ampex TBM Mass Storage System. The ATL was originally designed and marketed by Xytex Corporation of Boulder, Colorado.39 Early 1974 CalComp acquired the company, which was formally merged into XTX, a wholly-owned CalComp subsidiary in January of this year. ATL is a modular system with a basic configuration of a control unit, two storage units, a reel selector mechanism, and one automatic reel-mounting unit servicing one tape drive. This configuration is capable of storing 762 tape reels, and can be expanded by incremental addition of storage units and tape drives to accommodate 6250 magnetic tape reels and 32 tape drives. Under computer control the storage system automatically retrieves requested tapes, mounts them on the self-threading tape drives for system use, and dismounts and refiles them upon job completion. A complete inventory of status, usage, and location information for all tape files is maintained.

Ampex's random access terabit memory utilizes standard 2-inch-wide video tape recorded in a block format to provide up to 350 billion bytes of data on-line at a cost of about .0001 cent per bit.33,41 Each block is identified by a unique address allowing block-address searches, forward and backward, at 1000 inches per second. The system is in two parts: a data storage section composed of the transport modules, transport drivers, and data channels, and the control section with its storage control processor for system control and data channel processors to control data transfer between the TBM and the host computers. Each transport module includes two transports and has an 11-billion-byte capacity; a TBM system can have up to 32 transport modules, and with up to six transport drivers up to six concurrent accesses are possible. Each data channel unit performs independent read and write operations at a rate of 700 kilobytes per second. With three data channel units, the system maximum, six simultaneous read/write commands yield throughput of 4.2 megabytes per second. Switching matrices allow any transport to be accessed by any driver and data channel, and provide flexibility for dynamic reconfiguration and off-line maintenance of part of the system. The TBM is capable of operating independently of host processors; when used with host computers, the system can either stage data to shared disks or route the data directly to host channels.

The availability of two additional mass storage sys-
tems is questionable at this time. These two are the Precision Instrument trillion-bit laser-based mass storage System 190, a follow-on to their UNICON system which is installed on ILLIAC IV, and the Grumman Mass tape system, presently under reevaluation by its developers. System 190s had been ordered by the Social Security Administration, and by Holifield National Laboratory for ERDA Technical Information Center applications, before the company went into receivership. Refinancing plans have recently been announced, and it is now probable System 190 will be marketed. Characteristics of these two systems, as well as those of the IVC-1000 video tape recorder being adapted by TI for the GFDL ASC, have been included in the Table V mass storage system summary.

ALTERNATE STORAGE TECHNOLOGIES

Alternate storage technologies bridging the classical memory access gap between main memory and the peripheral storage devices, and at the same time, offering the per bit cost of the rotating disks and drums, have been the object of continuing research. During the past five years three areas in which there have been significant development efforts are: charge-coupled devices (CCD), bubble domain technology, and electron-beam addressed memories. The first two have been described as belonging to the "moving the bits to the sensor" philosophy, while the third applies the "moving the sensor to the bits" approach.

The CCD is, basically, a shift register for analog signals made in the form of a string of MOS capacitors. CCD memories, being serial in nature, are block-oriented rather than bit-oriented. Primary incentive for CCD memory development is its potential low cost derived from higher packing density and the inherently simpler fabrication. One drawback is the long access time associated with the serial nature of CCD technology. At this year's National Computer Conference, Fairchild described their CCD 450 9216-bit storage which is organized as 1024 9-bit bytes. The unit is viewed as a possible storage unit for portable terminals where its byte format and low power features can be exploited. Throughout the past five years magnetic bubble memories have been envisioned as a technology which is just two to three years away. Their most attractive characteristic is their non-volatility. Like CCD technology, the bubble domain systems offer low power consumption and high density per chip. By November of last year prototype bubble memory systems had been constructed by three companies, and Rockwell presented three illustrations of the technology at the NCC. One application was as a spacecraft tape recorder replacement, the second as an alternative to a tape cassette or floppy disk in a data logging device, and the third example was a block-organized memory for a data processing system. Access time quoted for the 64K-1024K, 16-bit, block-organized memory was 0.5 to 1 ms at a 0.05 cent-per-bit price.

Electron beam technology which dates back to first-generation computer memories, is once again showing promise. General Electric's Research and Development Center is presently building 32-million-bit BEAMOS (Beam-Addressed MOS) memory modules in pilot quantities. The BEAMOS module consists of a memory plane and electron-beam accessing system enclosed in a glass envelope; it has an access time of 30 ns and a transfer rate of 10 megabits per second. A "matrix electron lens" with 289 lenslets is used to direct the cathode-ray-tube beam to read, write, or erase at precise sites on the four silicon storage chips of the memory plane. Each of the chips holds 8 million bits. In a multimodule system, 16 or more tubes can be linked to provide a 512-million-bit or greater storage capacity. Data transfer rates of 160 megabits per second could be realized by accessing a 16-module system in parallel. Cost of the electron-beam addressed memory system is estimated to be in the .02 to .1 cent/bit range.

PERIPHERAL AND INPUT-OUTPUT EQUIPMENT

Although the industry has been actively seeking an all-electronic auxiliary memory, this has not seemed to discourage efforts in disk technology. New products introduced include the Storage Technology 8800 "super disk" with 800 megabyte capacity and the CDC 819 high-capacity disk subsystem with a 412-million-character capacity. Delivery of the 819, already incorporated in the STAR systems, is scheduled for August. This disk has an average access time of 50 ms, 8.3 ms average latency, and a transfer rate of 6.2 million characters per second. IBM and the IBM-compatible manufacturers continue to turn out the 3330 200-megabyte disks and the Winchester 3340 with its 25 ms average access time. Electronic News reported in May that disk drive shipments by U.S. firms were expected to reach 1.2 billion dollars this year, and tape drive shipments 1.3 billion. The ANSI 6250 magnetic tape standard will soon be out for public review and comment. This tape will become and remain a high-volume product due to its high data rate, low cost, and interchange capability.

Three I/O product areas projected for growth are high-speed printers, intelligent terminals, and floppy disks. Both Honeywell and IBM have introduced non-impact, high-speed printers. Livermore has had two of the Honeywell printer subsystems, which use Honeywell 716 minicomputers as controllers, in use off-line for over a year. Each 12,000-18,000 lpm unit has a read-only memory character generator which prints up to 192 characters using an electrostatic technique. Cost of the Honeywell subsystem is $162,120. In April of this year IBM announced a printer system that combines laser and electrophotographic techniques to
print up to 13,360 lpm on plain paper. It may be purchased for $310,000, and first customer shipments are scheduled for the third quarter of 1976. The 3800 can be attached to any channel and can print up to 225 characters, in four character sets at a time, on any of 50 page sizes. Characters can be produced in 12 to the inch, and 15 to the inch, as well as in the standard 10 to the inch size. A number of standard character fonts are included. Xerox markets a 4000 lpm page printer, known as the 1200, which is available on a rental basis only; the cost is $1500/month with a monthly page charge of 11 mills each for the first 100,000 pages, 7 mills each for the next 200,000, and 4 mills for each page thereafter. UNIVAC is rumored to be working on a 14,000 lpm laser printer, and at NCC Canon distributed literature on their off-line 1000 to 4000 lpm laser beam unit. Paper costs for the equipment vary as shown in Table VI.

Reports on terminals have predicted a rise from fewer than 200,000 in 1970 to almost 5,000,000 by 1980. LSI technology coupled with the growing trends to communications-based systems and distributed-function architecture make even that estimate appear conservative.

Floppy disk drive sales are expected to show a five-fold increase between 1975 and 1980. Applications of floppy drives are primarily in data entry systems, intelligent and point-of-sale terminals, and as minicomputer and microcomputer peripherals. The disk holds up to 1898 128-character records and is a very inexpensive memory unit; today's prices vary between $4.50 and $8.00 and reductions can be expected as market volume increases.

### NETWORK AND COMMUNICATIONS ACTIVITY

The network and communications area is the area destined to receive the most attention from the computer manufacturers in the next five years. An IEEE Computer Society glossary defines a computer network as an interconnected group of independent computer systems which communicate with one another and share resources such as programs, data, hardware, and software. Under this definition most of today's computer facilities can be classified as networks. With data traffic in the United States growing at an annual rate of 35 percent, computer manufacturers have become increasingly committed to the development of

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**TABLE V—Summary of Characteristics of Mass Storage Systems**

<table>
<thead>
<tr>
<th>Host interfaces</th>
<th>AMPEX</th>
<th>CALCOMP</th>
<th>CDC MSS</th>
<th>IBM MSS</th>
<th>PI 190</th>
<th>GRUMMAN</th>
<th>IVC-1000</th>
</tr>
</thead>
<tbody>
<tr>
<td>IBM 360/370, IBM 360/370</td>
<td>IBM 360/370</td>
<td>IBM 370</td>
<td>IBM 370</td>
<td>IBM 370</td>
<td>IBM 370</td>
<td>IBM 370</td>
<td>IBM 370</td>
</tr>
<tr>
<td>CDC, DEC</td>
<td>CDC</td>
<td>CDC</td>
<td>CDC</td>
<td>CDC</td>
<td>CDC</td>
<td>CDC</td>
<td>CDC</td>
</tr>
<tr>
<td>Capacity:</td>
<td>350B bytes</td>
<td>762-6250 reels</td>
<td>16B byte increments</td>
<td>35B-472B bytes</td>
<td>16B byte increments</td>
<td>128B bytes</td>
<td>11.8B byte increments</td>
</tr>
<tr>
<td>Media:</td>
<td>2&quot; video tape on 10½&quot; reel</td>
<td>½&quot; tape on 10½&quot; reel</td>
<td>2.75&quot; tape in plastic cartridge</td>
<td>3&quot; tape in plastic cartridge</td>
<td>rhodium-coated mylar strip</td>
<td>1/8&quot; tape in cartridge</td>
<td>1/2&quot; video tape on 12½&quot; reel</td>
</tr>
<tr>
<td>Unit capacity:</td>
<td>11B bytes/ module (module=2 reels)</td>
<td>3420 tape</td>
<td>8M bytes</td>
<td>35B-472B bytes</td>
<td>50.4M bytes</td>
<td>200M bytes</td>
<td>36M bytes</td>
</tr>
<tr>
<td>Unit cost:</td>
<td>$150/reel</td>
<td>$15/cartridge</td>
<td>$20/cartridge</td>
<td>$20-$25/strip</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Recording:</td>
<td>transverse VTR, block-addressable</td>
<td>longitudinal</td>
<td>longitudinal</td>
<td>helical VTR</td>
<td>laser beam</td>
<td>file-addressable</td>
<td>helical VTR</td>
</tr>
<tr>
<td>Access time:</td>
<td>search 1000 lps</td>
<td>11 to 14 sec</td>
<td>5 sec</td>
<td>3 to 8 sec</td>
<td>7 to 10 sec track access: 220 ms</td>
<td>avg 5 sec</td>
<td>max 15 sec</td>
</tr>
<tr>
<td>Data rate:</td>
<td>4.2M bytes/sec (6 channels)</td>
<td>1.23M bytes/sec</td>
<td>86K bytes/s from disk</td>
<td>86K bytes/s from disk</td>
<td>440K bytes/s</td>
<td>100K bytes/s single file</td>
<td>1M bytes/s</td>
</tr>
<tr>
<td>Price:</td>
<td>$400,000 to $700,000</td>
<td>$70,000 to $250,000</td>
<td>$700,000 to $400,000</td>
<td>$700,000 to $400,000</td>
<td>$4.5 million (16B system)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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**TABLE VI—A Comparison of Available High-Speed Printer Subsystems**

<table>
<thead>
<tr>
<th>Honeywell</th>
<th>IBM</th>
<th>Xerox</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology:</td>
<td>Electrostatic</td>
<td>Laser</td>
</tr>
<tr>
<td>Speed (lpm):</td>
<td>12,000-18,000</td>
<td>up to 13,360</td>
</tr>
<tr>
<td>Paper-use fees:</td>
<td>$2.61-$2.31/1000</td>
<td>$2.30/1000</td>
</tr>
<tr>
<td>Purchase price:</td>
<td>$162,120</td>
<td>$310,000</td>
</tr>
<tr>
<td>Rental:</td>
<td>$3667 minimum</td>
<td>$7,344</td>
</tr>
</tbody>
</table>

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coordinated hardware and software systems for communications-based information networks.

IBM's effort to provide a single uniform environment for data communications is identified as Systems Network Architecture, or SNA. Digital Equipment Corporation calls its DECNET software a set of tools to allow intersystem communication, and CDC has opted for the title Network Communications System (NCS) to describe a set of hardware and software being produced to accomplish the four processing functions:

1. interfacing one or more host computers;
2. interfacing a great number of terminals, often of widely varied use and manufacture;
3. routing data between its sources and its destinations;
4. interfacing, within the host computer, between user programs and external communication equipment.

The manufacturers are employing state-of-the-art technology and distributed-processing concepts in implementing communications subsystems to perform some of the functions previously assigned the central processor, such as communications management, data formatting, device control, and even application processing. In addition, they are defining the system software protocols for interfacing. SNA software elements defined include: Virtual Telecommunications Access Method (VTAM) to manage the connection and disconnection of terminals to application programs; NCP, the Network Control Program, to perform tasks associated with physical network requirements; and SDLC, the data transfer protocol defining the format for data exchange between two network nodes. NCP can be resident in a programmable communications controller.

DECNET utilizes three protocols, as well. The first, DAP, for Data Access Protocol, is designed to allow programs on one node of a network to use the I/O services of other nodes; the second, the Network Services Protocol, handles the routing of messages within or between systems; and the third, DDCMP, Digital Data Communications Message Protocol, serves as the data transfer, or link, protocol. Burroughs recently released a Burroughs Data Link Control (BDLC) designated as that company's data transfer protocol. The next step is to get all computer manufacturers to agree on common protocols. It appears adoption of an ANSI standard for data link control is about a year to a year and a half away. Until such a standard is adopted the incompatibility of communications hardware and software products will deter network growth. Once the bit-oriented data transfer level standard has been accepted, standards for the higher-level network protocols should be forthcoming.

SNA hardware to date consists of terminals and communications controllers, some general-purpose and others dedicated to a specific industry, or application.

Any new IBM system line, such as FS, is expected to be communications-based. CDC's first step in NCS hardware development was their 2550 Host Communications Processor (HCP) designed to interface terminals to a host computer, such as a CYBER 170. The HCP hardware includes a 16-bit microprocessor and is scheduled for delivery the latter half of this year.

In addition to the prospects of networking capabilities originating with the computer manufacturers, the Argonne, Berkeley, and Brookhaven laboratories are scheduled to complete connections to the ARPANET this year, and the first commercial packet-switched carrier is expected to begin service to customers in a seven-city operation soon.

Four years ago when Jack Worlton concluded his presentation it was with the thought that the long-awaited computer revolution was still a way off. His criterion for determining the advent of such a revolution required that the computer effectively penetrate to a large fraction of the private homes in our society. At such a time he felt it would be valid to speak of a computer revolution, and not until then, and he speculated that maybe this could happen by 1984. It will not be long before the microprocessor, incorporated in washing machines, automatic dryers, etc. will have done just that! By 1984, a personal computer equipped with keyboard/CRT, hard-copy device, and floppy disk could be available for under $500. With corresponding advances in information processing network technology, it will at some point become unprofitable to collect people in office buildings simply to talk to each other and pass papers. Given suitable computing and communications media, work of this nature can be done, possibly more effectively, on a distributed basis by people working at home. This "cottage industry" concept has some interesting social consequences, not the least of these is a reduction in the consumption of energy, which is in short supply, through increased information processing capability, which appears to have no perceivable limit. Indeed, the very existence of the human species is proof that information processing "power" does have survival value!

ACKNOWLEDGMENTS

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From the collection of the Computer History Museum (www.computerhistory.org)
REFERENCES


38. CONTROL DATA Mass Storage Facility, Control Data Publication 201.197, April 1975.


