An adaptable, modular data-collection system suitable for scientific experimentation — Analog to digital transformation, short-term digital storage, formatted digital tape-recording, and computer entry of experimental data

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ABSTRACT *

This paper describes an adaptable, modular data-acquisition system suitable for the collection of experimental data in a form readily adapted to subsequent digital computer entry and analysis. The system utilizes voltage-to-frequency conversion of an input analog signal over precisely regulated timing intervals. The digitized data is initially stored in shift-registers and later digitally formatted and digitally tape-recorded. The recorded data is read by a complimentary tape reading system and entered into a mini-computer for subsequent analysis and long-term storage. The digital formatting technique permits unambiguous definition and recovery of each data word as the tape is read.

Adaptations of this system necessary to accommodate variations in the length of each data-word and the number of words per message block are discussed.

Commercially available TTL integrated circuits and modular components are used in the design of this system.

INTRODUCTION

Scientific experiments often require a means of rapidly collecting and storing analog experimental data in a form readily adapted to later digital computer entry and analysis. Although commercial systems are available, individual systems better suited for the particular experimental configuration can be constructed with relative ease and at significantly reduced cost by using readily available TTL and CMOS integrated-circuits.

The data collection system described in this paper evolved from a desire to carry out electrophysiological experiments aimed at further characterizing the membrane charge movement phenomena in single, skeletal muscle cells (Schneider, M. F. and Chandler, W. K., 1973). A Digital Equipment Corporation PDP-8/E minicomputer was available for off-line analysis. Therefore, an interim means of storing the data for later computer entry was needed.

This paper describes an adaptable, modular data-collection system suitable for the collection of experimental data. The description is divided into four logical segments (Figure 1): (1) Data transformation using voltage-to-frequency conversion, and static shift-register storage of the digitized data, (2) Formatting of the stored, digital data using a Universal Asynchronous Receiver-Transmitter (U.A.R.T.), in preparation for tape-recording, (3) Digital tape-recording, and, (4) Reading and computer entry of the digitally tape-recorded data.

DATA TRANSFORMATION

The process of analog-to-digital conversion of the experimental data was simplified by using a voltage-toto-
frequency (V/F) converter module (Anadex Instruments, Inc. Model 1700-5044-00). The converter produces TTL/DTD compatible output frequencies of 0.1-1.0 MHz that are directly proportional to input D.C. voltage signals of 0-10 V.D.C. The linearity of the converter is better than 0.01 percent of full-scale, and its output responds virtually instantaneously to changes in input voltage. Experimental input D.C. voltages of ±100 mV in amplitude are amplified to a level commensurate with that of the V/F converter by an instrumentation amplifier (Analog Devices, Inc. Model AD520J) with externally adjustable gains of 1, 20, 50, or 100, and adjustable reference levels.

Voltage-to-frequency converters require less complex wiring for data transmission than do conventional analog-to-digital converters; only a single line is needed for a serial pulse-train. A clock signal and a counter at the receiving end are used to encode the pulse train. The process results in an analog-to-digital conversion and time-integration of the input signal. This was particularly desirable for later data analysis (Figure 1).

The output pulses of the V/F converter were counted by three cascaded four-bit binary counters (SN 74193) for externally adjusted intervals of 0.1, 0.5, 1.0, 2.0, 5.0, or 10.0 milli-seconds. Timing pulses, which had been buffered to TTL levels, were generated by a gated, pulse train output channel of a digital stimulator (Digitimer Ltd., Hertfordshire, England, Model 4030). When the binary counters for the V/F converter output receive a timing signal, the following sequence of events occur (Figure 2): (1) The input to the counters from the V/F converter is disabled, (2) The twelve-bit binary number presently in the counters is transferred to a digital (12 X 256)-bit storage register (NS 5055), (3) The binary counters are cleared, (4) A Master-Event-Counter is advanced by one count, and (5) The input to the V/F counters is again enabled. These five steps occur within 3.8 micro-seconds. By repetition of this sequence, a total of 256 sequential data points are sampled during any collection interval, (e.g. one oscilloscope sweep).

A Master-Event-Counter circuit serves to control two distinct sequences (Figures 1, 3, and 4): (1) The actual digital transformation of the analog data and the static storage of 256 digital data points, and (2) The digital formatting and then digital tape-recording of the previously collected 256, twelve-bit binary data words.

In conjunction with an initializing SYNCH pulse, CT1 and CT2 (cascaded four-bit binary counters SN 7493), and FF1 and FF2 (dual J-K flip flops with clear SN7473) are cleared. This sets QFF2 to logic high and enables the Master-Event-Counter and the sequence of events necessary to digitally transform and store the experimental data signal, as previously described. After 256 data points have been sampled, QFF2 toggles to logic high enabling the sequence of events required to format the 256 twelve-bit binary data words, and to initialize and consummate the
taping process. After taping of all 256 data words has been completed, FF2 again toggles setting QFF1 to logic high. This blocks any further timing pulses and blocks all counters until another SYNCH pulse is received.

Although independent and variable clocks are used to collect the data and to format and tape the data, the control logic segment assures that only a single Master-Event-Counter pulse is generated for each twelve-bit binary data word collected and for each original twelve-bit data word transmitted by the U.A.R.T. to the tape-recorder.

Although the data-collection system is designed specifically for the digital transformation and taping of 256 twelve-bit binary data words, it is easily adapted to any multiple of $2^n$ points by simply changing the Master-Event-Counter, the length and/or width of the shift-register buffer, and the number of bits per data word as may be appropriate for the resolution desired.

**FORMATTING OF THE STORED DATA WORDS**

A Universal - Asynchronous - Receiver/Transmitter (U.A.R.T.) in half-duplex mode was used to ensure the competency of the data interface between the 256 word shift-register buffer and transmission to the digital tape-recorder. The transmitter section of the U.A.R.T. (Texas Instrument Co, Model TMS 6011NC) accepts the parallel data from the shift-registers, converts it to serial form and generates a start, parity, and stop (1 to 2) bit(s) for each original twelve-bit binary data word. The data word length (5 to 8 bits long), the baud rate (0 to 200 KHz.), and the sign of a parity bit are externally selected. The formatting function and parity generation of the U.A.R.T. allow for unambiguous definition of each data word when reading the data tape and for the detection of dropped bits.

To transmit one twelve-bit word from the shift-registers to the tape-recorder, two ten-bit data words are sent by the U.A.R.T. Each word is formatted as shown in Figure 5. Each half (six bits) of the original twelve-bit data word is concatenated to an indicator bit. The indicator bit is used to indicate whether we have the front-half or the back-half of the original twelve-bit data word; this is rechecked when reading the tape.

The U.A.R.T. clock, derived from an internal oscillator, runs at a frequency of sixteen times the baud rate. Successive divisions of the U.A.R.T. clock rate by sixteen (for the baud rate), by ten (signalling each half-word), and then by two (denoting complete transmission of the two halves of the original twelve-bit data word), together with appropriate internal and external control logic allow for constant checking and control over the formatting and transmission processes. For each original twelve-bit data word, transmitted as two ten-bit, formatted U.A.R.T. words, the Master-Event-Counter is advanced by one count.

This configuration is easily adapted to any length data word by appropriate fragmentation of the data word into separate U.A.R.T. words, indicators bit(s), and appropriate division of the U.A.R.T. clock to form the clock pulse which serves as input to the Master-Event-Counter.

**DIGITAL TAPE RECORDING**

The core of the system is a MicroVox tape recording/reading unit (Micro Communications Corporation, Waltham, Massachusetts). There are two separate, hand-size units in this system: a WRITE unit and a READ unit. Each unit consists of a tape drive system, plus all the necessary data transfer and tape handling.
logic. The available lines are: CLOCK_IN, CLOCK_OUT, DATA, READY, END_OF_TAPE/BEGINNING_OF_TAPE, ON, and FAST_FORWARD. The internal CMOS circuitry of the MicroVox units provides true TTL-compatible logic interfaces (after appropriate buffering) to and from the data-collection system.

The WRITE unit is functionally a phase-lock loop (P.L.L.) (Figure 6). The P.L.L. functions as an electronic servo consisting of a phase detector, a low pass filter, and a voltage-controlled oscillator (V.C.O.). The V.C.O. enables the P.L.L. to synchronize or “lock” on the incoming clock signal. The clock signal (CLKIN) serves to clock in each bit of the word. As the phase of the clock signal changes, indicating a change in incoming frequency, the output of the phase detector will change just enough to keep the V.C.O. frequency the same as the incoming frequency. This allows the baud rate to be varied both dynamically and statically over a wide range.

In external-clock mode, the MicroVox WRITE system’s P.L.L. synchronizes with the leading edge of a user supplied clock-in (CLKIN) signal. This signal is derived from the successive division of the U.A.R.T. clock signal (16), described earlier. The WRITE system furnishes an externally available clock-out (CLKOUT) signal which is checked by the data-collection system to verify phase-locking quality. A modulator, internal to the WRITE system, then manufactures the waveforms of logic 1 and logic 0 which are written onto the tape in proper relation and synchrony with the formatted, serial data stream from the U.A.R.T. The MicroVox WRITE system can function over a range of 300 to 3200 bits/second.

This technique of pulse-coded modulation affords significant advantages over more conventional AM or FM recording methods: 1) A greater accuracy, (2) A significantly better signal-to-noise ratio (up to 90 db), (3) The capability for relatively long-distance transmission of the data without degradation since the digital signal can be regenerated with a very low probability of loss, and (4) The ability to computer process the information with virtually no modifications.

The tapes are continuous loop, one-track cartridges available in a variety of lengths. Since the tape is a loop, the physical end-of-tape (EOT) and beginning-of-tape (BOT) are the same. Provisions exist for detection of EOT/BOT as well as for file protecting each cartridge.

Transition of QFF2 of the Master-Event-Counter from logic low to logic high initializes the following sequence of events by the data-collection system leading to consummation of the WRITE function (Figures 6, 7): (1) Fast_Forward (FF) is set to logic 1 and ON to logic 0, thereby entering WRITE mode and accelerating the tape to speed. If initially stopped, the tape unit reaches speed within 60 milli-seconds. (2) The CLKIN signal derived from successive division of the U.A.R.T. clock is supplied. The MicroVox WRITE unit then furnishes an external READY (RDY) signal indicating that phase-lock and speed have been attained. This permits the external data-collection interface to transmit DATA to the recorder and allows the recorder to write the formatted DATA onto the tape. Had CLKIN not been supplied, the RDY signal would not be furnished and the data-collection interface would not permit the sending of DATA to the recorder. During such a state, the MicroVox WRITE unit would write bias onto the tape; this prevents mangle of message blocks and later allows the MicroVox READ system to start and stop between two consecutive message blocks. (3) Each data bit is clocked to the recorder by the CLKIN signal. There is a delay of approximately 1/2 CLKIN cycles between the occurrence of a CLKIN pulse and the actual writing of that particular data bit onto the tape.

In this fashion all 256 original twelve-bit data words (or 5120 U.A.R.T. bits) are transmitted. Upon com-

Figure 6—MicroVox WRITE unit: Functional block diagram reproduced with permission of Micro Communications Corporation

Figure 7—MicroVox WRITE system: Operating sequence
A formatted U.A.R.T. word is shown: s=start bit, 0-5 denote data bits, I=indicator bit (0 or 1), P=parity (odd or even), and st=stop bit (1 shown)
ploction of transmission, QFF2 of the Master-Event-Counter flips to logic low and in conjunction with a U.A.R.T. done flag, the CLKIN signal is discontinued. After 1½ bit periods, the time needed to write the last bit, RDY drops to logic 0. (4) The data-collection interface then sets ON to logic 0 and the tape dynamically brakes to a standstill.

The external data-collection interface provides the option of slowing to the EOT/BOT in Fast-Forward or slow mode (with CLKIN discontinued, FF=1, ON=1). EOT/BOT is optically sensed by the MicroVox WRITE and READ systems from two foil-reflectors spaced 3" apart and affixed to the tape.

During the writing of data, the occurrence of the first EOT applique causes the data-collection interface to finish writing only the current twelve-bit word (20 U.A.R.T. bits), and then the recorder is stopped. A new cartridge is inserted, and writing resumes under control of the Master-Event-Counter. However, in slew to EOT/BOT mode, the external interface stops the tape immediately after the second EOT applique in preparation for later reading or writing.

No modifications to either the data-collection interface controlling the MicroVox WRITE system (other than those already described) or to the tape unit itself are necessary to write any word-length, or number of words per data block.

DIGITAL TAPE READING AND COMPUTER ENTRY

The MicroVox READ system is specifically designed to read tapes produced by the MicroVox WRITE system. A high degree of cooperativity between the two units minimizes errors that could result from tape speed irregularities (e.g., wow and flutter), allows for writing and reading the same tape-wafer at widely different speeds, and results in simple adaptation of the tape units to a large number of external interfaces.

The instrumentation of the motor control functions (ON, FF, EOT/BOT) of the READ system are identical to those of the WRITE system; their functions are similarly controlled by the external data-collection interface. The bit density (b.p.i.) written on the tape, and the speed (i.p.s.) at which the tape is read determine the waveform presented to the READ head. Above a density of 800 b.p.i., the READ waveform is no longer usable. A dual-peak-detecting system, with a decent frequency response and insensitive to both amplitude and waveform, is used to allow for large variations in the amplitude, frequency, and shape of the waveform presented to the READ head.

To read a tape-wafer, the external data-collection interface is used to control the following sequence of events (Figure 8): (1) Fast Forward is set to logic 0 and ON to logic 1, thereby entering READ mode and accelerating the tape to speed. (2) The READY signal rises to logic 1 a full bit-interval before the first data bit is shifted to the external interface, allowing the maximum possible time in which to ready the external data interface. (3) A CLKOUT pulse is furnished by the READ unit approximately 5 µsecs. after each DATA bit is shifted. The process continues until modulation ceases, then (4) READY drops to logic low, and depending upon the states of the external interface and the computer program either the tape is stopped (ON to logic 0) or reading is continued (ON remains at logic 1).

**Data collection system—computer interface**

The use of the U.A.R.T. to format the data sent to the MicroVox WRITE system allows the data collection interface to unambiguously define the beginning, end, and origin (front-half or back-half of the original twelve-bit data word) of the words being read.

The start of each U.A.R.T.—word is defined as a transition of the READ system bit—output from logic high to logic low. This transition is detected by the external data-collection interface which is preset for the word-length, the parity (even or odd) and the number of stop bits (1 or 2) written.

Detection of a start-bit by the external interface enables the following sequence of events (Figure 8): (1) A word-length counter (SN 7490), parity generator (SN 74180), and a ten-bit series-to-parallel shift-register (SN 7496) are cleared. (2) Each bit of the ten-bit U.A.R.T.-word is clocked into the ten-bit series-parallel shift-register by the CLKOUT signal derived from the MicroVox READ unit. When a complete ten-bit U.A.R.T.-word has been shifted, (3) The word-length counter overflows, (4) Parity is checked and error flag(s) set as necessary, (5) Either the first-six or last-six bits of a twelve-bit parallel-in, parallel-out

![Figure 8](image-url)
buffer register (SN 74174) are loaded (with the data bits of the U.A.R.T. word) depending on whether the indicator-bit is a logic 1 or a logic 0, respectively. These five steps are repeated until the second U.A.R.T.-word has been received; then, (6) The data-collection interface flags the computer (D.E.C.—PDP-8/E) and a complete twelve-bit binary data word is read into core memory. (7) In response, the computer acknowledges receipt of the data word.

This process is continued until a total of 256 twelve-bit, binary data words (1 sweep) have been received and acknowledged by the computer. The controlling program then either stops the READ unit or continues the reading process as may be appropriate.

A Digital Equipment Corporation PDP-8/E minicomputer was used to control the read portion of the data collection system, and perform subsequent data analysis. During the READ cycle the data collection system communicates with the PDP-8/E through a D.E.C. M1709 omnibus interface module.

The computer was programmed in OS/8 Fortran IV. The actual control of the data-collection system is implemented by a RALF assembly language subroutine. The starting and stopping of the READ unit, the number of 256-word data blocks read, the handling of all error flags, and the transfer of the core resident data to Dectape for long term storage are all under program control. To maximize efficient use of storage, three twelve-bit binary data words are stored in both core and on Dectape in the space allocated for one Fortran floating point variable.

In subsequent analysis of such condensed data it is necessary to “float” each twelve-bit, binary data word into one Fortran floating-point variable. Each Fortran floating-point variable occupies 3 contiguous storage locations. This is accomplished by executing a call from the main FTN IV program to a specific RALF subroutine which floats a binary word. All program generated output destined for Dectape is recondensed before transfer.

The programs and interfaces are easily adapted to accommodate a variety of word-lengths, words per message block and other necessary control functions.

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