Interaction of technology and system architecture

Major hardware technology advances have and will have significant impact on system architecture by shifting feasibility constraints and causing new optimum structures to emerge.

This area develops the thesis that a number of very significant hardware technology advances are occurring or are about to occur. This, in turn, will result in significant changes in the: structure of software systems, productivity of systems, ease of use, operational practices, and range of applications of general purpose computing systems.

Some of the specific architectural areas considered are: multi-processors structures, storage hierarchy structure and control, firmware primitives for data-base applications, software architecture for memory and data management.

Sessions:

Professor Gerald Estrin, UCLA
Chairman—Introductory Panel Session

This introductory session will consist of two tutorial presentations pointing to the two following sessions. The first presentation will discuss major cost/density trends in main, disk and archival memories and how they are affecting system architecture and operating concepts for files, data bases and library systems. The second presentation will add major technology trends in processors and inter-connections and will discuss forms of Processor-Memory-Switch Architectures suggested by those trends.

Professor Stuart Madnick, MIT
Chairman—Paper Session—Processor Memory Switch (PMS) Architecture

Significant cost reduction advances in processor technology have now made multiple processor architectures economically feasible. In this session three specific examples are presented. The first uses an ensemble of up to 13 identical
processors to implement a highly-reliable communications switching node (ARPA IMP). The second addresses the problem of asymmetric task scheduling in a multiprocessor system with heterogeneous processors (HITAC 8700's and 8800's). The third describes a highly modular network of microprocessors connected together by a common ring-bus.

Noguchi, Kenichiro, et. al., Hitachi, Ltd., “Design considerations for a heterogeneous tightly-coupled multiprocessor system”
Toong, Hoo-min D., MIT, “Microprocessor-based multiprocessor ring structured network”

Dr. Jeffrey Buzen, Honeywell Information Systems, Harvard
Chairman—Paper Session—Data and Memory Management Architectures

The hardware capabilities provided by new technologies and the software requirements generated by new applications are exerting a powerful influence on memory subsystem architecture. This session will consider both hardware and software factors and will include discussions of the conceptual and architectural support of data base systems, the use of LSI technology to provide logical processing capabilities within a memory subsystem, and the use of microprocessors to support both memory subsystem hierarchies and software hierarchies in a uniform manner.

Glanz, Z. H., Thompson, P. M., University of Ottawa, “A data sorting system using high speed bus”
Madnick, Stuart E., MIT Sloan School, “Infoplex—A functional decomposition of large information management systems into a hierarchical microprocessor complex”

Mr. Richard P. Case, IBM
Chairman—Discussion Panel on Significance

The panel will consist of the three session chairmen plus one or two guests.