BEAMOS—A new electronic digital memory


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INTRODUCTION

BEAMOS, for Beam Addressed Metal Oxide Semiconductor, is a new technology for auxiliary memories based on an electron beam which reads and writes data on a simple unstructured MOS chip. It can store data for months with or without power.

This memory combines large data capacity, high data transfer rate and a highly flexible data format. BEAMOS use in data systems should result in significant savings in both hardware and software costs.

This technology also makes possible auxiliary memories with the ruggedness and non-volatility needed for military systems.

Static auxiliary memories such as cores or semiconductors become extremely expensive and decline in overall reliability when large amounts of storage capacity are required. This results in severe constraints for the designer of military information systems. BEAMOS memories provide an attractive alternative.

DESCRIPTION OF THE BEAMOS MEMORY

A complete BEAMOS memory consists of one or more BEAMOS modules, address and interface logic, control circuits, and power supplies.

A 32 million bit capacity was chosen for initial development because it was the most viable size for the applications envisioned. Lower capacity modules are relatively easy to design and build but have a higher cost per bit. Higher capacity modules provide less modularity in systems design, but on the other hand, have lower per bit component cost.

Physical description

The BEAMOS module, Figure 1, contains a memory plane and electron beam accessing system enclosed in a sealed, evacuated envelope. In military systems the module is shock mounted in a rugged outer shell.

Memory plane

Information is stored on the memory plane, Figure 4, which consists of four BEAMOS chips mounted on a baseplate. The essential structure is shown in Figure 2. It consists of a film of aluminum evaporated on a thin insulating layer, such as silicon dioxide, formed on a silicon diode. All layers are arranged in continuous, unstructured planes. The n and p type silicon layers are connected electrically to form a back-biased diode. The operating mode of the memory is controlled by the application of a voltage across the oxide layer. A positive 40 volt bias is applied to write and a negative 40 volts to erase. A read bias of zero volts allows many reads before rewriting. Destructive readout can be obtained with a negative 40 volt bias.

Electron beam addressing

The conventional way to address an electron beam to a given location in a field is through a single stage of deflection. The maximum number of addressable sites is determined by the accuracies of the deflection structure and the driving amplifier, and by the stability of the power supplies. A practical open-loop limit is approximately 1000 addressable sites along a line, and hence a million addressable spots in a square field. In the BEAMOS module, addressing of the electron beam to the memory sites is achieved in a special electron optical structure. This employs two stages of deflection, in combination with a unique matrix of small lenses. This array of lens/deflection systems, called the Matrix Lens, permits addressing a very large number of discrete memory sites with a single electron beam.

The complete electron optical system of the BEAMOS module is shown in Figure 3. The first digits of the address are applied to a digital-to-analog converter. This converter generates an analog voltage which is applied to the first deflection stage called a lenslet selector. This directs the electron beam into one of the small lenslets. A lenslet is simply a pair of aligned holes in two metal plates. A voltage applied between the plates produces an electron lens which focuses the beam to an extremely fine spot. In addition to its focusing capability, each lenslet has an individual deflection structure, integral with the matrix lens.
The second part of the digital address is applied to another digital-to-analog converter, producing a deflection voltage that is applied to this second deflection structure called a page selector. This structure directs the beam into the desired memory site within the lenslet field. The two deflection stages are effectively independent. Minor beam positioning variations in the first stage do not cause significant errors in the position of the bit site addressed. Figure 4 is a photograph of a Matrix Lens together with the memory plane. The grid structure is the page selector matrix.

Operating sequence

To record data in the module the following sequence is performed. First the address and operating mode are selected by simultaneously entering the lens and page addresses and switching in the desired oxide bias. This moves the beam to the beginning of the page. From this point the beam is stepped across the lenslet field one bit site at a time while the electron beam is synchronously turned on or off as required by the input data. An output signal is available from a read amplifier which can be monitored as a partial check on the write operation.

The sequence is the same for the other operations (read, destructive read, and erase), except that the electron beam is turned on at every bit site.

Signal life

The BEAMOS target stores data for a long time but not permanently. Thus it is necessary to rewrite the files occasionally whether they are used or not. This function can be carried out by reading the data into a block buffer and rewriting. Signal decay is very slow with the power off or with power on and zero or negative oxide bias values. With
power off, the measured signal is 90 percent of its initial value after five day storage and about 80 percent after one month. Decay is somewhat faster at positive bias. The decay characteristic is only slightly temperature dependent with variation of no more than +10 percent in signal level between -40 and +70°C.

The output signal from the module is also reduced slightly by each readout. After approximately 20 reads it must be rewritten. It is advantageous to operate the module such that several reads are always possible, so that re-read cycles can be used as a part of the error recovery strategy. Data refresh can be done after each read or when necessary, based on the readout signal level.

MEMORY SYSTEM CHARACTERISTICS

The BEAMOS module can be configured into memory systems which have a wide spectrum of characteristics. This design freedom results from the non-structured nature of the storage plane and the flexibility of electron beam addressing.

Data format

The data layout used in the BEAMOS module can be selected at the discretion of the systems designer. The page length can vary over wide limits, however, a guardband must be left between pages to assure that activity on one page does not affect neighboring pages. A guardband is also required between lenslets. There are no built-in restrictions on word length and redundancy can be included within the page as required for error control.

An example of a particular format based on a 8448 bit page is shown in Figure 5. Here each page occupies 24 data lines extending completely across the lenslet field. A
12 micron guardband is provided between pages and a 125 micron guardband between lenslets.

**System configuration**

Systems needing 32 million bits capacity require only a single module. In larger systems, multiple modules are used and advantage can be taken of the fact that much of the electronics can be shared among several modules, thus minimizing the cost per bit of the system. Figure 6 is a block diagram of a multimodule system in which the modules are addressed one at a time. In this configuration, the modules share the lens and page select amplifier, oxide bias circuitry, most of the digital electronics and the power supplies. This provides minimum per bit cost and maximum reliability with page access times in the 30 microsecond range and data rates up to 10 megabits/second. Data capacity for a 20 tube system would be at least 600 million bits.
In some systems, much higher data rates are desirable to minimize service time. This can be provided by accessing modules in parallel. That is, all, or several, modules are simultaneously addressed to the same location and each writes or reads a part of the total page. Again much of the electronics is shared among the modules but since more digital electronics is required the cost per bit can be expected to go up somewhat.

This type of system can have a 30 microsecond access time, 600 million bit capacity and data transfer rates up to 200 megabits/sec.

Access time

Access time, the time required to move the electron beam to the beginning of a page, is fundamentally limited by the transit time of the beam through the optical system, about 30 nanoseconds. The practical electron beam access time limit is imposed by the switching and settling time of the deflection amplifier driving the capacitance of the all electrostatic lenslet and page selectors. This can be in the range of a few microseconds.

The time required to change the bias of the oxide when switching from one operation to another (i.e., read to write) requires a longer time because the relatively large oxide capacitance must be charged through the resistance of the n-layer in the memory plane. This can be accomplished, with time for the disturbance caused in the readout amplifier to die out, in about 30 microseconds.

Thus, the access time can be a few microseconds for successive calls of the same operation and up to 30 microseconds if an operation change is involved.

Data rate

The recording data rate is determined by the beam current available. In the present modules this is 10 megabits/sec. Considerably less beam current is required to read, making it possible to read at higher rates. Target frequency response is not a limiting factor. At higher read rates fewer reads can be made before the data has to be rewritten because more beam current is required. At 10 megabits/sec about 20 reads are possible, while at 100 megabits this would be reduced to six.
Service time and some system consequences

A meaningful number describing the speed of a memory system is service time. This is the average time between the acceptance by the memory of a new command and the earliest time the next command can be accepted. In many applications the service time of the file equipment can have a dramatic effect on the performance of the total system. As an example of this, consider a transaction processing system in which a database is shared among many users. The system has a CPU and a working memory with space for the file management software and eight partitions for transaction programs.

Requests for CPU and memory time come in on a random basis from the users and the required programs are brought in from the file and assigned a portion of the main memory. The programs are executed in turn until they are completed or an operation which requires considerable time is encountered, for example, an input/output command or a memory access. When this occurs the operation is initiated and the CPU goes on to the next transaction. When transactions begin to come in at a rate approaching the average processing rate, queues build up and the waiting time may become unacceptably long or the number of transaction partitions exceeded.

The software for such a system must be very complex to cope with all eventualities. A particularly troublesome situation occurs when two transactions which are resident in main memory call for access to the same file; one to modify it and the other to read it. In this case it may be necessary to roll both transactions back to their initiation to decide whether the modification or read should occur first.

This kind of system has been studied by computer simulation to determine the effect of service time on its performance. The results are dependent upon the capabilities of the CPU and file memory and upon the nature of the transactions in more detail than can be discussed here, but Figure 7 illustrates what can happen.

These calculations were made for a real system operating on a transaction mix typical of those occurring in a manufacturing plant automation data system.

With a file service time of 40 milliseconds which is typical of disk devices the operation of the system is limited by the file memory. Only three to four transactions/second can be accommodated before unacceptable delays begin to occur. At this point all of the memory partitions are occupied with transactions in process, greatly increasing the chances for conflicts in the use of the data base.

If the service time is decreased to 0.44 milliseconds, as would be possible with a BEAMOS memory, the capacity of the system is increased to the point where over 20 transactions/second can be processed. The transaction rate would be three times that achievable with the slower file with only one memory partition occupied. This means that transactions could be processed serially in order of arrival, with a consequent simplification in data base protection and operating system software and with less main memory.

SUITABILITY FOR MILITARY APPLICATION

A version of the BEAMOS memory is presently under development for U. S. Army ECOM and assessments of its suitability for military environments look very promising.

Military environment

A major advantage of BEAMOS for use in a military environment is that it is all electronic, has no moving parts and is completely sealed. No parts are especially sensitive to vibration and the most important section in controlling beam position, the matrix lens/target assembly, is very rugged. Tests of this component suggest that it can easily be applied in typical aircraft vibration environments. By using familiar isolation techniques, application can be extended to very severe environments. Tests of the BEAMOS storage plane over the range -50°C to +70°C indicate that charge storage is not greatly affected by temperature and while there are some changes in target characteristics, it is possible to design the system to accommodate them. The matrix lens/target assembly is made of materials with matching coefficients of expansion so that variation from -40 to +70°C should produce less than 0.1 micron variation in the position of the addressing beam.

The memory module requires a magnetic shield to protect against external fields, but a shield weighing about 10 pounds will accommodate fields up to 10 gauss. Considerably lighter shielding will suffice in less severe environments.

The BEAMOS memory plane is especially tolerant of ionizing radiation since it depends on high radiation levels for its operation. Ionizing radiation equivalent to 10^9 Rads (Si) will cause no more than 10 percent reduction in signal
level. No permanent radiation damage has been observed up to $6 \times 10^7$ Rads. Neutrons will generate permanent damage but $10^{14}$ neutrons/cm$^2$ are required to cause significant reduction in signal level.

Military packaging

An important consideration in most military equipment is physical size and power consumption. A packaging study has shown that a single module BEAMOS memory can be packaged in a volume of 2-3 cubic feet and will require about 250 watts of power. The study assumed packaging techniques similar to those used in aircraft.

Reliability

The mean operating time between failures is a part of most military equipment specifications. It is useful to make an estimate of what might be expected in a memory of this type. A single module system was considered and by making a component count and applying component failure rate data from the Military Standardization Handbook$^4$ the following MTBF figures were determined.

<table>
<thead>
<tr>
<th>Component</th>
<th>MTBF</th>
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<tbody>
<tr>
<td>Digital Circuits</td>
<td>30,000 hours</td>
</tr>
<tr>
<td>Analog Circuity</td>
<td>36,000 hours</td>
</tr>
<tr>
<td>Power Supplies</td>
<td>20,000 hours</td>
</tr>
<tr>
<td>Resultant MTBF of</td>
<td></td>
</tr>
<tr>
<td>Electronics Circuits</td>
<td>9,000 hours</td>
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</tbody>
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It was assumed that the module itself would be replaced on a preventive maintenance schedule. The electron source$^5$ was a barium dispenser cathode.$^6$ At the cathode loading employed the dispenser cathode used in these devices can be expected to show only 10 percent drop in emission in 40,000 hours of use.$^5$ A 20,000 hour replacement period was selected, and assuming random failures of 20 percent prior to replacement, the combined MTBF for the electronics and the BEAMOS module is calculated to be 8,000 hours. This compares very favorably with other memories of this size and would be even more favorable for multimodule systems.

DEVELOPMENT STATUS

The 32 million bit BEAMOS memory module is being built in pilot quantities. These modules are being tested and evaluated in a computer controlled test system. Modules have been operated at a data density of 40 million bits per square inch which produces a module capacity of 32 million bits. They have been tested at data rates of 10 megabits/second and access times of 30 microseconds. Data storage time between refresh cycles can be as long as 120 hours.

MEMORY COST COMPARISONS

Estimates of the cost of a BEAMOS memory including the analog and digital electronics have been made and they compare favorably with competing technologies. The systems price will vary depending upon the number of modules used but is expected to be in the 0.02 cent per bit range for the present module size and density. The price can be expected to decline with future developments into the 0.001 cent per bit range.

POTENTIAL FOR IMPROVED PERFORMANCE

The BEAMOS concept has considerable potential for improvement with continued development. Operation of the memory plane with the matrix lens optics has been achieved in an experimental laboratory configuration at 100 million bits/in$^2$.

Improvements in the electron optics can also increase the addressable target area in a module. A theoretical study supported by experimental evidence has demonstrated that 10 square inches of target space can be addressed at 160 million bits/in$^2$. This provides a data capacity of over $1 \times 10^9$ bits per module.

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REFERENCES


3. Raymond, R. C., private communication.


