The sessions on storage provide a review of recent activity in mass storage along with an update on the several technologies which are contending for a place in the storage hierarchy. These two sessions are complemented by two sessions concerned with systems and reliability aspects. On the latter issue, the application of algebraic coding theory to both data transmission and data storage is investigated. An extensive piece of theoretical and experimental work is reported and hardware implications for mass storage are considered.

Very large mass storage devices have been the subject of increasing industry attention as a result of new activity by manufacturers. Particular attention is given to the internal architecture as well as the software aspects of these storage systems. Additionally, the session addresses the operational requirements for such devices in order that they may solve the major physical data handling problems in a large computer installation.

There is a high degree of activity in many industrial laboratories searching for better technologies than those which currently reside in a hierarchy. An entire session will be devoted to understanding the state of development of the novel technologies. These include bubbles, CCD’s, super-conductors, holographic storage, and electron-beam storage. Each of these technologies offers different cost and system design trade-offs. Each has particular advantages which motivate its ultimate promise. The goal of this session is to give a comprehensive and balanced view of these, in order that their long-term promise can be assessed.

The last session is a panel addressing the system applications of advancing storage technology. As new storage function is provided and as old storage function becomes less costly, the systems architect has the opportunity to reassess his old trade-offs and consider new system structures. The panel will range from such issues as the opportunity for new technology in the access gap between memory and electromechanical storage to new system structure opportunities allowed by a very inexpensive memory removed from the central processor. Our goal is to produce a dialogue which will allow both the technologist and the system architect to better exploit the new memory technology.