A planarity algorithm based on the Kuratowski theorem*

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INTRODUCTION

In the layout of integrated circuits and printed circuits, one often wants to know if a particular electrical network is planar, i.e., can be imbedded in the plane without having any line crossing another line. Our algorithm, when given a finite graph $G$ can decide if $G$ is planar. The algorithm was implemented in Fortran together with the Cycle Generation Algorithm for Finite Undirected Linear Graphs of Gibbs and used extensively to test the planarity of a large number of graphs. The distinguishing characteristic of this algorithm is its conceptual simplicity and its ease of implementation on a computer. The computer program took but a few days to write and debug.

In contrast to some of the recent work on the same subject, this planarity algorithm is a direct application of the Kuratowski Theorem. It is based on the observation that a Kuratowski graph can be spanned by the union of two of its circuits. This algorithm can be used in conjunction with existing algorithms which generate all the circuits of a given graph $G$ to test the planarity of a large number of graphs.

The paper begins with the necessary notation and definitions. This is followed by the presentation of the algorithm and a few brief comments.

Definition 1: Let $V$ be a finite non-empty set and $E \subseteq \{\{v_1, v_2\} \mid v_1, v_2 \in V \land v_1 \neq v_2\}$, then $G = \langle V, E \rangle$ is a finite undirected graph without loops or multiple edges, or more simply, a graph.

Definition 2: A subgraph $G' = \langle V', E' \rangle$ of a graph $G = \langle V, E \rangle$ is a graph where $V' \subseteq V$ and $E' \subseteq E$.

Definition 3: Let $G = \langle V, E \rangle$ be a graph and $X$ a non-empty subset of $E$, then $S_{G}(X) = \langle V', X \rangle$, the subgraph of $G$ spanned by $X$, is the subgraph of $G$ where $V' = \{v \mid v \in V \text{ and for some } x \in X, v \in x\}$.

Definition 4: A non-empty subset $C$ of edges of a graph $G$ is a circuit (or cycle) of $G$ if $S_{G}(C) = \langle V', C \rangle$ is such that for each $v \in V'$, there are exactly two elements of $C$ which contain $v$, and $C$ does not properly contain any other circuit of $G$. $C$ is said to be of length $k$ if it has $k$ elements.

Definition 5: The class of all subgraphs of $G$ which are spanned by the union of two distinct circuits of $G$ will be denoted by $TC(G)$, i.e.,

$$TC(G) = \{S_{G}(C_1 \cup C_2) \mid C_1 \text{ and } C_2 \text{ are distinct circuits of } G\}$$

Definition 6: Let $G = \langle V, E \rangle$ be a graph, we define an open simple path of $G$ inductively. $(\emptyset, \{e\})$, where $e \in E$, is an open simple path. If $(V', E')$ is an open simple path, then so is $(V' \cup \{v\}, E' \cup \{e\})$ where

1. $e \in E - E'$
2. $v \in V - V'$
3. there is some $e' \in E'$ such that $v \in e \cup e'$
4. for all $v' \in V', v' \notin e$.

Figure 1 shows two examples of open simple paths.

Definition 7: Let $(V, E)$ be an open simple path of $G$ and $(V_1, E_1) = S_{G}(E)$. Then $V_1 - V$ has exactly

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two elements, \( u \) and \( v \), and we say \( u \) and \( v \) are connected by the open simple path \( (V, E) \).

Definition 8: Two open simple paths \( (V', E') \) and \( (V'', E'') \) are disjoint if and only if \( V' \cap V'' = E' \cap E'' = \phi \).

Definition 9: A \( K_5^* \) graph is a graph which can be constructed by taking a set \( V \) of five vertices and connecting every pair of distinct elements of \( V \) by an open simple path such that these open simple paths are pairwise disjoint.

Definition 10: A \( K_{3,3}^* \) graph is a graph which can be constructed by taking two disjoint sets, \( V_1 \) and \( V_2 \) of three vertices each and connecting every member of \( V_1 \) to every member of \( V_2 \) by an open simple path such that these open simple paths are pairwise disjoint.

Figure 2 shows examples of the simplest \( K_5^* \) and \( K_{3,3}^* \) graphs.

Note that every \( K_5^* \) (every \( K_{3,3}^* \)) graph may be obtained from that of Figure 2 by replacing the set of edges by a set of pairwise disjoint open simple paths.

Theorem (Kuratowski): A graph is planar if and only if it does not have a subgraph which is a \( K_5^* \) or a \( K_{3,3}^* \) graph.

Observation (J. R. Buchi): A graph \( G \) is planar if and only if \( TC(G) \) does not contain any \( K_5^* \) or \( K_{3,3}^* \) graphs.

In fact this follows from the Kuratowski Theorem because each \( K_5^* \) and each \( K_{3,3}^* \) can be spanned by two circuits. The union of the two circuits in Figure 3 span the \( K_5^* \) graph of Figure 2.

The union of the two circuits of Figure 4 span the \( K_{3,3}^* \) graph of Figure 2.

We are now ready to state our algorithm which may be programmed in conjunction with a circuit generation algorithm, for example, the algorithms of Gotlieb and Corneil, and of Gibbs to determine whether or not a graph \( G \) is planar from its vertex-adjacency matrix (vertices vs. vertices). Given two circuits \( C_1 \) and \( C_2 \), let \( S_G(C_1) = \langle V_1, C_1 \rangle \) and \( S_G(C_2) = \langle V_2, C_2 \rangle \). In brief, steps 2 and 3 of the algorithm check to see if \( S_G(C_1 \cup C_2) \) is a \( K_5^* \) graph. If \( S_G(C_1 \cup C_2) \) is not a \( K_5^* \) graph, \( V_1 \cap V_2 \) has more than five elements, and \( C_1 \cap C_2 \) has more than two elements, then steps 5 through 8 of the algorithm essentially eliminate all the vertices of degree 2 of \( S_G(C_1 \cup C_2) \) and then check to see if the resultant graph is \( K_{3,3} \)—the simplest of the \( K_{3,3}^* \) graphs.
ALGORITHM

1. Given a graph $G$, generate all the circuits of length five or greater.

2. Given two circuits $C_1$ and $C_2$, let $S_G(C_1) = (V_1, C_1)$ and $S_G(C_2) = (V_2, C_2)$. If $V_1 \cap V_2$ has exactly five elements and $C_1 \cap C_2 = \phi$, go to the next step, otherwise, go to step 4.

3. Trace $S_G(C_1)$ in one direction and let $(v_1, v_2, v_3, v_4, v_5)$ be the elements of $V_1 \cap V_2$ ordered in this cyclic order. Check to see if these elements can be placed in a cyclic order $(v_1, v_3, v_5, v_4, v_2, v_6)$ when $S_G(C_2)$ is traced. If the answer is "yes," $S_G(C_1 \cup C_2)$ is a $K_5^*$ graph and $G$ is non-planar. If the answer is "no," go to step 9.

4. If $V_1 \cap V_2$ has more than five elements and $C_1 \cap C_2$ has more than two elements, go to the next step, otherwise, go to step 9.

5. Form the vertex-adjacency matrix $M = (m_{ij})$ of $S_G(C_1 \cup C_2)$ as follows:

$$m_{ij} = \begin{cases} 
0 & \text{if } \{v_i, v_j\} \notin C_1 \cup C_2 \\
1 & \text{if } \{v_i, v_j\} \in C_1 - C_2 \\
2 & \text{if } \{v_i, v_j\} \in C_2 - C_1 \\
3 & \text{if } \{v_i, v_j\} \in C_1 \cap C_2 
\end{cases}$$

6. Go through the matrix row by row once, doing the following:

- If row $k$ has exactly two non-zero entries (note that these must be equal), say $m_{ki}$ and $m_{kj}$ are not zero, then add $m_{ki}$ to $m_{ij}$ and $m_{kj}$ and set $m_{ki} = m_{kij}$, $m_{kj} = m_{kji}$, and $m_{ij} = 0$. Otherwise, go to the next row.

7. After the last row, if there remain exactly six rows with non-zero entries and each of these rows has exactly three non-zero entries, go to step 8, otherwise, go to step 9.

8. The resultant matrix is the vertex-adjacency matrix of a cubic graph $G' = (V', E')$ with six vertices. Let $C_1'$ be the circuit of $G'$ consisting of the six edges labeled by a "1" or a "3" and let $C_2'$ be the circuit of $G'$ consisting of the six edges labeled by a "2" or a "3." Note that $S_{G'}(C_1' \cup C_2') = G'$. Let $(v_1, v_2, v_3, v_4, v_5, v_6)$ be the elements of $V'$ in the cyclic order obtained by tracing $S_{G'}(C_1')$ in one direction with the edge $\{v_1, v_2\} \in C_1' \cap C_2'$. Now start with $v_1$ and go to $v_2$ and continue tracing $S_{G'}(C_2')$. If the resultant cyclic order of $V'$ is $(v_1, v_2, v_3, v_4, v_5, v_6)$, then $S_G(C_1 \cup C_2)$ contains a $K_{3,3}$ graph, otherwise, go to step 9.

9. The graph $G$ is planar if there are no more pairs of circuits to be considered. Otherwise, select another pair of circuits $C_1$ and $C_2$ of $G$, and go to step 2.

CONCLUSION

It may take the algorithm a relatively long time to find out that a large planar graph is indeed planar, but the relative ease with which the algorithm can be programmed should render it suitable for testing a small number of graphs or graphs that do not have a large number of circuits. Although a relatively large computer was used in our implementation, the algorithm is simple enough to be implemented on a computer of almost any size. Step 1 (the generation of circuits) of the algorithm can be executed first and the generated circuits can be stored on some form of auxiliary storage. The check for planarity can then be executed separately.

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