INTRODUCTION

The computer industry is no doubt one of the most rapidly growing industries today. With the increase in computer usage, there is an increased demand to improve man's ability to communicate with the computer. The prime instrument of input communication today is a keyboard, and it appears that this will be true for some time in the future.

The requirements of today's keyboards are becoming more complex. Increased reliability and more flexibility to meet specialized demands are essential. Remote terminals are quite often operated by relatively untrained personnel and the keyboard must be capable of error-free operation for these people. At the same time it should be capable of high thru-put for the trained operator as will be used on a key tape machine.

Some of the limitations of existing keyboards are:

- Mechanical interlocks which reduce operator speed.
- Excessive service (increasingly important for remote terminals).
- Contact bounce and wear of mechanical switches.
- Non-flexible format.

Our general objective in developing the solid state keyboard was to overcome these limitations and still have a competitively priced design.

Keyboard organization

Before setting forth specific design objectives, some general comments may be helpful, depending on the reader's familiarity with this type of equipment. The purpose of a keyboard is to feed information into a digital computer by means of a binary code. An eight-bit parallel code is usually used. Two codes currently used are ASCII and EBCDIC and the keyboard design and construction must be such that any code can conveniently and economically be supplied. The output signal must be compatible with the solid state integrated circuits used in today's computers.

Specific design objectives

At this point, each key may be thought of as a simple switch, actuated by the position of a key plunger.

Human factors studies have helped establish the following for mechanical and tactile features of key operation.

Operate force: 2 to 5 ounces
Pretravel (before operate): .075 inches min. from free position
Release point: .040 inches min. from free position
Release point (R.P.) ≤ Operate point (O.P.) − δ
where δ = differential

Switching transitions should be "snap acting" or regenerative so that it will not be possible to hold a key in a position that will cause ambiguity at the output. Rise and fall times must be in the low microsecond range without any ringing or oscillation. The encoding electronics must be capable of blocking error codes when two or more keys are depressed.

Keyboard formats are quite varied, depending on the user's needs and preferences. This indicated that each key should be a separate module. Finally, the service life should be in excess of 10 million operations per key,
and low cost was given a priority second only to reliability.

The approach

From the outset, our thinking was slanted toward the development of an integrated circuit chip transducer for the key module. The powerful and still growing economic advantages of batch processing used in integrated circuit manufacture were considered essential to our stringent cost objectives. To fully exploit these advantages, it was desirable that the chip be complete in itself i.e., that it require no external components to accomplish its function. The latter cannot be added in batch fashion.

Several approaches to mechanical position detection without contacts were studied, based mostly on unique sensor effects available in a semiconductor such as silicon. Position control of an electric, magnetic, acoustic, or electromagnetic (including optical) field pattern is fundamentally involved. Hall effect sensing in a silicon device, including appropriate integrated electronics, and coupled with permanent magnet actuation, was singled out for detailed analysis, design and development.

This approach was eventually adopted for the solid state keyboard. The competing approaches mentioned above, though quite feasible, seemed to require more expensive packaging, or more expensive and less reliable field sources, or were known to require external components in the electronics. Magnetic actuation looked particularly attractive because it appeared that the sensor device could be integrated on the silicon chip along with associated electronics as well as allowing more freedom in package selection. Among the several galvanomagnetic effects present in semiconductors, we found that only the Hall effect in silicon is large enough to be useful in the low field (\(< 1000 \text{ Gauss}\)) region of interest.

The silicon chip that has been developed is described by the functional breakdown in Figure 1.

A circuit schematic is given in Figure 2, and a picture of the chip comprises Figure 3.

Some of the analytical and experimental investigations associated with this development are presented in what follows.

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**Hall effect characterization**

As many readers will already know, the Hall effect is old in scientific terms, having been discovered by Edward W. Hall in 1878. It is currently enjoying a renaissance of practical applications interest due mainly to advances in semiconductor technology. Two publications by A. C. Beer provide excellent general references. The Hall effect results directly from the Lorentz force on moving charge carriers, where the average motion is constrained in direction, as in a solid. This is illustrated in Figure 4. The Lorentz force creates a charge unbalance in the y-direction. The resulting
The Hall effect in a solid is a direct manifestation of the Lorentz force on moving charge carriers:

**Equation 1** shows an approximate Hall voltage expression for a homogeneous layer with predominately one type of carrier concentration.

\[ V_H = \frac{R_H IB}{10^8 t} \]  
\[ R_H = \text{Hall* coefficient} \approx \frac{1}{nq} \]
\[ n = \text{concentration (cm}^{-3}) \]
\[ I, B, V_H = \text{mutually perpendicular} \]
\[ t = \text{Thickness (cm)} \]
\[ B = \text{Gauss} \]
\[ V_H = \text{volts} \]
\[ I = \text{amperes} \]
\[ q = \text{charge on an electron} \]

Since most electronic circuits operate from a constant voltage supply, equation 2 below is more appropriate. It is straight-forward derivation* from equation 1 for a rectangular geometry.

\[ V_H = \frac{V_s u_n B W 10^{-8}}{L} \]  
\[ V_s = \text{supply voltage} \]
\[ u_n = \text{mobility (cm}^2/\text{v-sec}) \]
\[ W = \text{width} \]
\[ L = \text{length} \]

A factor less than unity has to be applied to equation 2 if the aspect ratio W/L is not smaller than unity. This is due to the shorting effects of the end contacts on the Hall field. One cannot increase the Hall voltage indefinitely by increasing W/L.

Equation 2 illustrates the important role of carrier mobility. In this respect, silicon is not a good material compared to, say, InSb or GaAs. However, one must go beyond equations 1 and 2 to include practical constraints of power dissipation, electrical resistance, range of impurity concentrations, and temperature variation of Hall coefficient. When this is done, silicon looks much better. Relating constant current and constant voltage modes of operation to semiconductor processing, observe that thickness and concentration (equation 1) are also the major processing variables that control resistor values in integrated circuits, and the expected tolerance is quite large. On the other hand, with constant voltage, only the mobility is process dependent, and it tends to be a weak function of concentration in the region of interest. Thus we expect and obtain much better reproducibility of Hall voltage with constant voltage excitation. This is gained at the expense of a higher temperature coefficient, however, due to the variation of mobility with temperature.

Assuming a field of 1000 Gauss to be available, straight-forward calculations using typical mobility and reasonable geometries showed that we could obtain a signal of about 30 millivolts with a five volt supply, and without exceeding typical power dissipation capabilities in IC chips.

Figure 5 shows an expression for total d.c. output voltage of a Hall element, including the effects of small loading at the Hall terminals. The characterization is entirely in terms of parameters measurable at the terminals. The offset voltage term, V_q, which is the open circuit output voltage with zero magnetization, is a very important parameter in this device. Economic restrictions ruled out the use of external resistors for adjustment of V_q. Its nominal value using IC technology depends mostly on contact geometry and sheet resistance uniformity in the conducting layer comprising the Hall element. Fortunately, very accurate geometries are possible using photolithographic techniques developed

* We assume "Hall mobility" and "conductivity mobility" to be substantially equal for the conditions of interest. The validity of this assumption, has been confirmed through private communication with Dr. G. D. Long, Honeywell Corporate Research Center.
If \((I_3 + I_4) \ll I_H\):

\[V_{34} = V_q + V_H - I_3R_3 - I_4R_4\]

\[V_q = \text{Offset Voltage}; \quad V_H = \text{Hall Voltage}\]

Figure 5—Hall element output voltage characterization

for IC fabrication. Variations in \(V_q\) can be caused by several factors, such as internal stress (through the piezoresistance effect) and temperature gradients. Regardless of the nature of the electronic circuitry that follows the Hall element, the variations in \(V_q\) must be much lower than the Hall voltage for adequate "signal-to-noise" ratio.

**Design—Process interrelationships**

As with any integrated circuit development, the circuitry, device physics, and process techniques are interdependent, and must be so treated. At the time the development was initiated it was considered essential for low cost objectives to use the epitaxial-diffusion, bipolar, NPN based, type of processing which was rapidly becoming an industry standard. MOS type processing was not sufficiently controllable to be seriously considered.

In an NPN type of bipolar structure, the collector layer has the lowest carrier concentration and highest mobility; it is the best choice for a Hall element. Hence the design approach was pursued on the basis of forming the Hall element simultaneously with collector regions for NPN transistors. The same isolation diffusion is used for defining the Hall element geometry. (The Hall element outline is faintly visible in Figure 3). Since this is a novel type of Hall element structure, some preliminary experimentation was conducted, confirming its feasibility and the accuracy of the preceding characterizations.

As to process considerations for the associated circuitry, the objective was to take advantage of conventional IC processing strengths, which lead to high yield results on the following:

1. High gain, accurately matched NPN transistors.
2. Low gain PNP transistors.
3. Accurate control of resistance ratios, but not absolute values.

Throughout the design-development cycle, extensive effort was devoted to achieving a simple design that is amenable to high yield processing, yet adequate for the intended function without external components.

**The trigger circuit**

The function of the trigger circuit is to accept the linear output (with or without linear amplification) of the Hall element and convert it to a binary or ON-OFF mode, with regenerative switching transitions and controllable hysteresis (or differential between the "turn on" and "turn off" operate points).

The trigger circuit we devised is shown in Figure 6. It is a variation on the Schmitt type of circuit. It may be implemented with just two resistors and two bipolar transistors. An approximate analysis aimed at providing insight into its general characteristics will be given here.

Assumptions used in approximate analysis:

a. The transistor model shown in Figure 6 applies. The most important feature of this model is that Shockley's law applies to the \(I_E - V_{BE}\) characteristic. This is well established for silicon planar bipolar transistors. Extrinsic resistances, collector conductance and all time dependent effects are omitted. The model requires active region operation, which is easily met.

b. \(I_E = I_E' = I\), a constant

c. \(I_E \ll I_C\) (high gain)

The static voltage control characteristics at the input base is of primary interest.

\[V_s = V_{ss} - V_{ss'} - I_C R_4\]  \(\text{(3)}\)

Using the above assumptions this becomes,

\[V_s = -\frac{KT}{q}\left(\ln \frac{I_E}{I_E'} + \ln \frac{1 - I_E/I}{I_E/I}\right) - (aIR_4) I_E/I\]  \(\text{(4)}\)
The first term of equation 4 represents the control characteristic of a conventional difference amplifier stage using the same assumptions noted above. The second term is the result of linear regenerative feedback. If this term has the appropriate magnitude, the transfer characteristic will have a negative resistance region that covers a few millivolts. The transfer characteristic may be easily observed on a curve tracer using a discrete component version of the circuit. One such observation is reproduced in Figure 7. The constant total emitter current condition is approximated in this version of the circuit by using an emitter resistor with voltage drop that is several times larger than the $V_{BB}$ voltage.

The nature of regenerative switching transitions may be reviewed in a number of references, particularly those dealing with tunnel diode circuits. Chapter 15 in Linvill and Gibbons' book is especially good. We will only note here that the trigger points depend exclusively on static parameters, and are given by the transition points from positive to negative resistance around any closed mesh of the circuit. Reactive effects, active device response time, etc., affect the speed of the switching transition, but not the fact of its occurrence. The trigger points are thus found by taking the derivative of equation 4, shown below as equation 5, equating it to 0, and simultaneously solving equations 4 and 5.

$$\frac{dV_B}{d(I_E)} = \frac{KT}{q(1 - I_E/I_B)} - \alpha I_{R_4} = 0 \quad (5)$$

A result from this approximate analysis is given below for one condition of regenerative feedback. The “ON” condition is defined as $T'$ conducting and $T$ off.

<table>
<thead>
<tr>
<th>$\alpha I_{R_4}$</th>
<th>Turn ON point $V_B$</th>
<th>Turn OFF point $V_B$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.130 volts</td>
<td>.069 volts</td>
<td>0.723</td>
</tr>
</tbody>
</table>

$$\frac{KT}{q} = .026 \text{ volts, and } I_s = I'_s$$

Our investigations showed that this circuit configuration could provide regenerative switching transitions with rather precisely defined trigger points and voltage transitions between trigger points of a few millivolts. The component requirements are well suited for integration, with critical performance depending on transistor matching and resistance ratios. Note that the transistor matching requirements are the same as for a good difference amplifier stage, with $V_{BB}$ matching to about $\pm 2$ millivolts. This is routinely done in IC's, due to close physical proximity, extremely accurate matching of geometries, and simultaneous processing.

**Output amplifier**

The output amplifier, consisting of a PNP stage driving an NPN Darlington, operates in standard saturated switching logic fashion. Its characteristics are relatively non-critical. The PNP is fabricated with a “lateral” geometry and its current gain is low. Static conditions for the OFF and ON states are as follows:

<table>
<thead>
<tr>
<th>INPUT</th>
<th>OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>OFF State $T'$ Off</td>
<td>Output voltage = 0 (with reference to—PNP base) supply)</td>
</tr>
<tr>
<td>ON State $T'$ On</td>
<td>Output voltage = supply voltage minus $(V_{CE \text{ SAT}<em>2} + V</em>{BE} + V_{BB})$</td>
</tr>
</tbody>
</table>

$V_{BE}$ SAT $V_{CE}$
As previously noted, a functional requirement is that there be no linear region in the output of the device, i.e., output voltages between the OFF and ON levels can only exist on a transient basis. This requires that the thresholds associated with the output amplifier operation be well within the negative resistance region of the trigger circuit control characteristic. The resistor \( R_2 \) is designed such that the value of \( I_C \) at the trigger circuit turn on point will not develop enough voltage across \( R_2 \) to forward bias the PNP base-emitter junction. The combined PNP-NPN gain requirement is such that the PNP stage saturates at a value of \( V_e \) that is below the trigger circuit turn off point. Resistor \( R_1 \) provides adequate margin against self turn-on in the Darlington stage under worst case temperature and gain conditions.

The output transistor has dual emitters and provides two isolated outputs. This aids in the encoding logic; in effect, part of that logic is included in the chip. This is an example of the economics possible when using IC technology, for the additional output adds virtually no cost to the chip.

An additional benefit of the solid state keyboard is that the output signal from the key does not require additional buffering to eliminate the effects of contact bounce. Switching times are in the low microsecond range and are free from ringing or oscillation.

Integration of sensor and electronics

Aside from the usual considerations of parasitic interactions within an integrated circuit, the special effects resulting from including the sensor in the IC chip constituted an interesting and novel aspect of this development. In general, we find more advantages than disadvantages in this approach and predict a growing trend toward “integrated transducer” semi-conductor devices. Inductance parasitics are virtually eliminated due to the extremely small dimensions. A potential source of ringing or oscillation in regenerative switching circuitry is thus avoided. For the same reason, noise pickup in the leads from sensor to electronics is minimized. High impedance leads to the outside world are avoided.

In the functional operation of this device, magnetization is applied over the entire chip. This has no effect on the electronics, as expected, for the resistors and transistors do not have any magnetic sensitivity in the magnetic field range of interest. The Hall element output, like a balanced bridge with matched temperature sensitive resistors, is sensitive to temperature gradients. This has to be taken into account in the output stage design and operation, and the thermal design of the package. The most troublesome parasitic encountered has been the stress sensitivity of the Hall element through the piezoresistance effect, previously mentioned, and this has been overcome by some special mechanical features in the chip-package design.

Chip specification

The specification is given in Table I. It is written as broad as possible to maximize the overall process yield.

Computer aided analysis

In the design of a product intended for the computer field, the utilization of computer-aided analysis seems especially fitting. When we avoid some of the simplifying assumptions used in the preceding approximate analysis, equations analogous to (4) and (5) become extremely cumbersome. Their simultaneous solution to obtain operate and release points becomes humanly intractable; a computer program was written to obtain such solutions.

Performance of the device was studied as a function of several independent parameters.

1. Supply voltage
2. Transistor gain, matched and prescribed mismatch
3. Emitter junction saturation current, matched and prescribed mismatch
4. Resistor and resistor ratios \( R_1, R_4/R_1 \)
5. Offset voltage, \( V_q \)

Space does not allow presentation of this analysis and results. The reader may contact the authors if interested. The computer-obtained results have been of great value in guiding the design and the design-process relationship. Figure 8 shows the effect of gain and

![Figure 8—Effect of gain and gain mismatch](image-url)
gain mismatch. We note that performance becomes essentially independent of transistor beta in the range above 50. With these results, a realistic process gain specification minimum of 30 was established.

**Temperature characteristics**

The dependence of operate and release points on temperature for a typical device is shown in Figure 9, based on experimental data. The slope of the curves is roughly accounted for by the expected temperature dependence of mobility. However, second order effects in the circuitry have a certain influence, not completely analyzed at this time. First order temperature effects in the circuitry are eliminated by use of matching and ratioing techniques.

**Packaging the chip**

Upon examining the economics of integrated circuits, it becomes apparent that much of the cost of commercial integrated circuits is in chip packaging rather than the chip itself. It was necessary, therefore, to develop a low cost, reliable packaging technique suitable for magnetic operation.

In developing such a package there are many parameter trade-offs that must be made in order to arrive at an optimum configuration. In most standard chip packaging approaches the chip is eutectically bonded to a metal leadframe or header. The metal is normally Kovar which closely approximates the thermal expansion of the silicon chip. Since this device was to be magnetically operated, Kovar is not desirable because it is ferromagnetic. On examining the non-magnetic metals and alloys, it was evident that there were none with the proper thermal coefficient of expansion. Therefore, it was necessary to find another method of holding the chip. The approach selected was to allow the chip, in essence, to float in a non-rigid potting material. This is accomplished in the following manner: A leadframe is stamped from phosphor bronze, inserted into a mold, and transfer molded with a rigid plastic leaving a cavity for the chip and access to the ends of the leadframe as is shown in Figure 10. It should be noted that the cavity for the chip is entirely plastic.

The chip is inserted into the cavity and the four wires are ultrasonically bonded between the pads on the chip and the leadframe. At this point, the chip is held in place by the four wires. The final packaging operation is to fill the cavity with a silicone potting material, which has a very low viscosity in the uncured condition, and it completely encapsulates the chip including the reverse side. Figure 11 shows the chip in its cavity prior to being potted.

In order to minimize the cost of this packaging approach, it was necessary to design so that wire bonding could be automated. This was accomplished in the following manner. The wafer is sawed into chips with an abrasive slurry, rather than use the normal scribe and break process. The sawing produces chips with square edges and with dimensions controlled to within ±.001 inches. The chip cavity is made only slightly larger than the maximum chip size; hence the location of the pads on the chip relative to the leadframe is rather precisely controlled. This allows the wire bonding machine to be mechanically aligned, rather than require the operator to make a visual alignment for each bond. It should also be noted from Figure 3 that the pads on the chip are large—(by integrated circuit standards)—approximately .010" square.
Without a eutectic bond to provide heat transfer between chip and package, it is necessary for heat transfer to occur through the aluminum wires and the silicone potting material. By using .002" diameter wire the thermal resistance is 355 degrees Centigrade per watt, unpotted. The potting material further reduces this to 266 degrees Centigrade per watt, which is quite comparable to the standard plastic dual in-line package.

**Magnet actuation**

If a bar magnet is moved along its axis perpendicular to the plane of the Hall element, the normal component of flux will vary with the magnet movement according to the curve shown in Figure 12. Since the curve runs asymptotic to the zero flux axis, a slight change in the release point of the chip would require a large change in the movement of the magnet to reach the release point. This is not desirable. If two magnets are used and are magnetized as shown in Figure 13, the flux versus gap position curve will tend to be sinusoidal. This is desirable if the total travel of the magnet assembly can be limited to the nearly linear portion of the curve. Since the flux required for both operate and release points is positive, the negative portion of the curve would not be used. By inserting the two magnets in a "U" shaped shunt and magnetizing them in place with a specially shaped magnetizing fixture, it is possible to produce the curve shown in Figure 14. The result of this is to move the majority of the sinusoid above the zero flux axis. Figure 14 also shows the magnet assembly and the shape of the poles on each of the magnets.
The magnets are made of polyvinyl chloride filled with barium ferrite. This combination produces an extremely stable, yet low cost, permanent magnet material. The shunt is soft iron which increases the magnet efficiency and helps to reduce the effect of stray magnetic fields. The chip package is made as thin as possible to reduce the air gap. The magnet assembly with the chip package is shown in Figure 15. Referring to the specification on the chip, and relating these to the flux versus position curve, it is possible to establish the operate and release points of the key, as shown in Figure 16.

Table I—Chip specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Minimum</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operate Point (OP)</td>
<td>300</td>
<td>750</td>
<td>Gauss</td>
</tr>
<tr>
<td>Release Point (RP)</td>
<td>100</td>
<td></td>
<td>Gauss</td>
</tr>
<tr>
<td>Differential (OP − RP)</td>
<td>150</td>
<td></td>
<td>Gauss</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>4.75</td>
<td>5.25</td>
<td>Volts</td>
</tr>
<tr>
<td>Supply Current (OFF Condition)</td>
<td>15</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Output Voltage (ON) @ 5V supply</td>
<td>3.4</td>
<td>3.6</td>
<td>Volts</td>
</tr>
<tr>
<td>Output Voltage (OFF) 5000 ohm load</td>
<td></td>
<td>0.25</td>
<td>Volts</td>
</tr>
<tr>
<td>Output Current (ON) (each terminal)</td>
<td>10</td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

Reliability test results

A variety of environmental tests have been made on the key chip integrated circuit, packaged as noted herein. In addition to tests on functional performance on conventional chips, chips with special metallization patterns were prepared and packaged, such that junction characteristics and Hall element output could be measured directly. This allows a more sensitive indication of incipient degradation than does functional performance. Table II describes tests on four lots of devices. The results are in keeping with the reliability
Table II—Reliability test results

<table>
<thead>
<tr>
<th>No. of Devices</th>
<th>Type of Test</th>
<th>Environment</th>
<th>Time</th>
<th>Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>30</td>
<td>Functional,</td>
<td>Normal Office</td>
<td>15 months</td>
<td>No failures</td>
</tr>
<tr>
<td></td>
<td>magnetic actuation</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>Functional,</td>
<td>75 to 100 deg. F.</td>
<td>4630 hrs.</td>
<td>No failures</td>
</tr>
<tr>
<td></td>
<td>magnetic actuation</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>Hall element (V&lt;sub&gt;e&lt;/sub&gt;)</td>
<td>70 deg. C.</td>
<td>1000 hrs.</td>
<td>Maximum variation of 2%</td>
</tr>
<tr>
<td>6</td>
<td>Collector junction</td>
<td>70 deg. C.</td>
<td>1000 hrs.</td>
<td>No change</td>
</tr>
<tr>
<td></td>
<td>V&lt;sub&gt;CBO&lt;/sub&gt; @ 10 μA</td>
<td>90% R.H.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

expected of semiconductor devices, when designed, processed and packaged properly. These tests are continuing and others are being initiated.

Mechanical assembly

The magnet assembly is inserted into the key plunger which is shown in Figure 17. The plunger magnet assembly is guided in the key housing by large area guides. We have shaped the top of the plunger and the inside of the two-shot molded button so that the button is press fitted directly into the plunger, avoiding the conventional adaptor pin. In addition to lower cost this provides the advantage of a low keyboard profile.

The chip package is inserted into slots in the housing which hold it in the gap of the magnet assembly. Two small tangs on the bottom of one side of the magnet shunt hold the return spring in place. This spring is designed to provide the two to five ounces of operating force under minimum stress conditions, assuring long life without getting weak.

The key module, shown in Figure 18, is inserted into a mounting rail. The module snaps into the rail, which has clearance holes for the leads of the chip package to extend through it and be soldered into a printed circuit board. The mounting rails are welded to the end mounting bracket and the entire assembly is riveted to a PC board as shown in Figure 19. The printed circuit board provides the electrical connection between the key modules and a second PC board. The latter contains the electronics for encoding, the strobe signal, and the electrical interlock which prohibits an error code generation when more than one key is depressed.

CONCLUSION

The solid state keyboard uses a new switching concept which capitalizes on the inherent reliability and low
cost of integrated circuits. The output of this device is compatible with the integrated circuits used in computers.

The keyboard is deliberately made modular so that it can be adapted to special key formats and codes. It provides an electronic interlock instead of the usual mechanical one, and as a result allows higher speed operation.

While the keyboard is different in many respects, it has maintained those industry standards which have been substantiated by human factor studies such as key stroke and force, key location, and the key layout in the touch typing area.

ACKNOWLEDGMENTS

The development of the solid state keyboard has been possible through the enthusiastic support and dedicated efforts of many people in our respective organizations. We could not hope to fairly cite individual contributions within acceptable space limits here. We also appreciate the consultation provided by other research and engineering groups in our Company.

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