An integrated MOS transistor associative memory system with 100 ns cycle time

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INTRODUCTION
Since the announcement of the development of a technique for using MOS transistor integrated circuits as associative memory cells,1 128 words of 48 bits per word associative memory has been experimented and engineered.

This paper deals with characteristics of a fully integrated associative memory chip utilizing MOS transistor technology and a method of a multimatch resolving in the associative memory system.

The associative memory chip contains 4 associative memory cells encapsulated in a 14-lead flat package.

This associative memory cell is designed so as to operate at a cycle time of 100 ns with standby power less than 100 \( \mu W \) and power dissipation less than 1 mW (peak) during the interrogate operation.

The advantage of using these associative cells is that they will provide economically practical cells with large scale integration and also they will be useful to realize a large capacity associative memory because of their small power dissipation.

This report is composed of two sections. In the first section, theoretical analysis and experimental results of operating speed of an integrated MOS transistor associative cell are shown. The second section describes the circuit configuration and the method of multimatch resolving of an associative memory matrix.

Associative memory cell
A four bit fully integrated associative memory chip is shown schematically in Figure 1 and a photograph of the associative cell is also shown in Figure 2.

The flip-flop is constructed with the MOS transistors \( Q_1, Q_2, Q_3, \) and \( Q_4 \). The MOS transistors \( Q_3 \) and \( Q_4 \) are used for read and write operations, and the MOS transistors \( Q_1 \) and \( Q_2 \) for interrogate operation. MOS transistors \( Q_5 \) and \( Q_6 \) are used as load resistors of \( Q_1 \) and \( Q_2 \), and have characteristics equivalent to resistance of about 3 M\( \Omega \). \( Q_1 \) and \( Q_2 \) have the highest mutual conductance.

The operation of the associative cell will be described qualitatively at first. The “1” and “0” digit lines are usually held at +5V, the “1” and “0” interrogate lines and the work-sense line at +18V, and the word line at +15V. Then, if \( Q_1 \) is on and \( Q_2 \) is off (the flip-flop stores a “1”), \( Q_5 \) conducts when the voltage level at the word line is shifted from +15V to -5V for reading, resulting in a digit sense current output at the “1” digit line and no output at the “0” digit line. On the other hand, if the flip-flop stores a “0”, \( Q_6 \) conducts resulting in a digit sense current output at the “0” digit line. Figure 3 shows the timing of waveforms during read and write cycles. During the write cycle the voltage level at the selected word line shifts from +15V to -5V for reading, resulting in a digit sense current output at the “1” digit line and no output at the “0” digit line. On the other hand, if the flip-flop stores a “0”, \( Q_6 \) conducts resulting in a digit sense current output at the “0” digit line. Figure 3 shows the timing of waveforms during read and write cycles. During the write cycle the voltage level at the selected word line shifts from +15V to -5V and at the same time the write information is given on the “1” or “0” digit lines as shown in Figure 3.

For an interrogation of “0”, the voltage level at the “0” interrogate line is shifted from +18V to +16V. If the flip-flop stores a “0”, it is so designed
that $Q_s$ is off, therefore no current is supplied to the word-sense line. If the flip-flop stores a “1”, a large output current appears on the word-sense line since $Q_s$ is on.

For an interrogation of “1”, large output current is supplied to the word-sense line through $Q_7$ when the flip-flop stores “0”.

In short words, this associative cell generates a signal on the word-sense line through $Q_7$ when the flip-flop stores “0”.

In short words, this associative cell generates a signal on the word-sense line only when there is a mismatch between the state of the flip-flop and the interrogate information. And no signal appears when the associative cell is not interrogated (don’t care).

The feature of this associative cell is that the power dissipation at $Q_7$ or $Q_s$ can be made small when mismatch signal appears in the interrogate operation. Namely, the characteristics of $Q_7$ and $Q_s$ are chosen properly so as to give a small voltage between drain and source of $Q_7$ or $Q_s$ and to give a large current to the word-sense line.

The current detector composed of an NPN transistor in grounded base configuration is capable of detecting the current given to the word-sense line kept at +18V.

In the worst case, namely in case that a mismatch signal is given by one bit out of 48 bits in one word, the current given to the current detector is to be about half of the current generated at an associative cell.

Another feature of this associative cell is that the mutual conductance of $Q_1$ and $Q_2$ is chosen to be three or four times of that of $Q_5$ and $Q_6$. This relationship is the necessary condition to prevent from the disturbance of flip-flop in the read mode.

Since $Q_5$ and $Q_6$ are actually equivalent to 3 MΩ resistor, as mentioned already, they give almost no effects on the switching characteristics. High-speed write operation is realized by MOS transistors $Q_4$ and $Q_6$.

Now provided $Q_1$ is off and $Q_2$ is on, let us estimate the switching speed of this associative memory cell in the case of shifting the voltage of “1” digit line from +5V to $+V_a (+V_a > +5V$) and the voltage of word line from +15V to some value $V_w$, resulting in on state of $Q_5$ and $Q_6$. In order to make $Q_1$ on state, first $Q_5$ is made off by increasing the voltage of node A. When $Q_5$ gets off state, $Q_6$ conducts and hence the voltage of node B decreases. When the voltage of node B gets to some value, $Q_1$ becomes on state. Therefore, after $Q_1$ reaches sufficient on state, write operation of “1” is finished by restoring the voltage of “1” digit line from $+V_a$ to +5V and word line from $V_m$ to +15V. Estimation is made in two steps; in the first step calculation is done for the time $t_1$ required to make $Q_5$ off as a result of increasing the voltage of node A by $Q_6$, and in the second step the time $t_2$ required to make $Q_1$ on as a result of decreasing the voltage of node B by $Q_6$ is calculated. In order to calculate $t_1$ and $t_2$ the characteristics of P-channel MOS transistor are given by the following equations.2

$$i_d = k_p \left(2(V_g + V_T) - V_d - V_d'\right) \quad V_d > V_g + V_T$$

where

- $i_d$: drain current
- $k_p$: constant
- $V_g$: gate voltage for source
- $V_T$: absolute value of threshold voltage
- $V_d$: drain voltage for source

**Read cycle**

- +15V
- +5V (Vs)
- -5V (Vs)

**Write cycle**

- +15V (Vb)
- +5V (Vb)

Figure 3 – Timing of waveforms at read and write cycles
The following gives the time $t_1$ required to shift the voltage of node A from an initial value $V_0$, which is specified by the threshold voltage $V_T$, to the voltage $V_{cc}-V_T$ to make $Q_2$ off.

$$
t_1 = C_A \int_{V_0}^{V_{cc}-V_T} \frac{dv}{i_{ds}}
$$

$$
t_1 = \frac{C_A}{2K_p(V_{w}-V_a+V_T)} 1_n
$$

$$
\left[ \frac{(V_{cc}-V_T-V_a)(2(V_w+V_T)-V_a-V_0)}{(V_a-V_0)(2(V_w+V_T)+V_T-V_a-V_{cc})} \right]
$$

where symbols are as shown in Figure 1 and 3 and $i_{ds}$ is the drain current of MOS transistor $Q_2$, and $C_A$ is the total capacitance of node A. $V_{cc}$ is shown in Figure 1.

Now the time $t_2$ required to shift the voltage of node B from $V_{cc}$ to the initial value of node A is given by

$$
t_2 = C_B \int_{V_{cc}}^{V_0} \frac{dv}{i_{ds}}
$$

$$
t_2 = \frac{C_B}{2K_p(V_{w}+V_T-V_b)} 1_n
$$

$$
\left[ \frac{(V_b-V_0)(2(V_w+V_T)-V_b-V_{cc})}{(V_b-V_{cc})(2(V_w+V_T)+V_T-V_b-V_0)} \right]
$$

where $i_{ds}$ is the drain current of MOS transistor $Q_6$, and $C_B$ is the total capacitance of node B.

Therefore switching time $t_w$ is given by

$$
t_w = t_1 + t_2.
$$

Figure 4 shows the relation between $t_w$ and $C_A$ ($=C_B$), provided $K_p = 0.05$ mA/V$^2$, $V_T = 5V$. It is easily found from Figure 3 that $t_w$ becomes 30 ns in case $V_w = -5V$, $C_A = 10$ PF, and $V_o = +7V$ and thus the switching time is fast enough to achieve a cycle time of 100 ns.

Figure 5 shows the experimental results of measurement of this associative cell.

Initially, an associative cell is placed in the “1” state by the coincidence of the first word pulse and the “1” write digit pulse, which are shown by traces (a) and (b), respectively. Then, the second word pulse to read the state of the cell follows. The trace (g) corresponding to the second word pulse shows the output for a “1” condition. The cell is next interrogated by the “0” interrogate pulse of trace (d), and a mismatch signal is generated as shown in trace (f). Then the cell is interrogated by the “1” interrogate pulse of trace (e). There is no mismatch signal found in trace (f). The “0” write digit pulse of trace (c) and the third word pulse are used to change the cell from the “1” state to a “0”. The cell is again interrogated by “1” and “0” interrogate pulses. Figure 5 shows a sequence of the above operations.

To improve the characteristics in the read operation after the write operation, some investigation is being performed. One of the methods is that $Q_7$ and $Q_8$ are used for interrogate and read operations, while $Q_5$ and $Q_6$ are used for write operation only. With this modification, a certain improvement would be expected.

**Associative memory system**

As mentioned already, the integrated MOS transistor associative cell has low power dissipation characteristics in interrogate operation. Moreover, since word matching signals can be obtained from associative memory matrix during the entire interrogate operation, the interrogate operation and sequential read operation of matching words are simultaneously performed until the entire multimatch resolving process is finished. Therefore, multimatch resolving can be done in high-speed by use of integrated MOS transistor associative cells and high-speed peripheral circuits. Of course the most important function is to attain a high-speed operation, low cost and simple multimatch resolver.
Although some methods have been reported about multimatch resolving\textsuperscript{3,4}, this paper describes a different approach in the multimatch resolving.

As shown in Figure 6, general sequence of events taken place is that firstly an arbitrary interrogate information activates interrogate drivers and the interrogate information is compared with the stored information in an associative memory matrix. Signals indicating matching words are fed into the detector matrix for dividing X and Y components. These components are stored in the X and Y-multimatch resolvers and the priority is given to each resolver. Based on X and Y configurations, a specific word driver is activated for the selection. The process continues under the priority control until X and Y-singlematch detectors detect the end of current interrogation.

The details in our system will be described below with an example.

The associative memory matrix consists of 128 words of 48 bits per word with associative memory cells which are described in section 1. This memory matrix provides the matching signals on the word-sense lines corresponding to matching words to the detector matrix after receiving interrogate information.

![Figure 5 - Results of measurement](image)

![Figure 6 - General block diagram of MOS transistor associative memory](image)
The detector matrix shown in Figure 7 has an essential function for multimatch resolving. The matching signals generated by each word-sense line of 128 words are given to the 128 AND gates which are divided into 16 groups as shown in Figure 7. Each group has 8 AND gates.

Logical diagrams of the Y-multimatch resolving circuits and X-multimatch resolving circuits are shown in Figure 8 and 9 respectively.

Initially, flip-flop FY-1 in Figure 8 will be set by some of word matching signals m₁ through m₈ in the group 1 when Y set pulse shown in Figure 8 is enabled. Also at the same time flip-flops FY-2 through FY-16 will be set by some of the word matching signals in the group 2 through 16 respectively. Thus set state of FY-1 through FY-16 shows that at least one matching word exists in the corresponding group. The flip-flops FY-1 through FY-16 in Figure 8 and the flip-flops FX-1 through FX-8 in Figure 9 are modified J-K flip-flops and consist of CML integrated circuits as shown in Figure 8. This flip-flop has the feature that it is set at the front edge of a set pulse given to S terminal and is reset at the trailing edge of a reset pulse given to R terminal. Y control shown in Figure 8 is normally in “1” state. Thus the priority in the order of Y₁, Y₂, Y₃, ..., Y₁₆ is established by the Y control.

It is assumed that, for example, at least one of matching signals in the group 2 and the group 11 are provided, and then FY-2 and FY-11 are set, but only
Figure 8 - Logical diagram of Y-multimatch resolver
Y₂ is in “1” state for processing the matching signals m₉ through m₁₆. When the entire processing in the group 2 is over, then Y control temporarily becomes “0” state to reset FY-2 and the priority control moves down to FY-11. Therefore, for the above example, when Y₂ is in “1” state, the states of m₉ through m₁₆ are stored in flip-flops FX-1 through FX-8 respectively. The states of 8 matching signals in the one group with the highest priority will be stored in FX-1 through FX-8 by enabling X set pulse as shown in Figure 9. Suppose FX-3 and FX-8 are set by m₁¹ and m₁₆. Thus the states of FX-3 and FX-8 show the matching words in the group 2. The word clock in Figure 9 establishes the priority in the order of X₁, X₂, X₃, ..., X₈. The overall timing chart for the above example is shown in Figure 10 and the first word clock comes, and then X₃ as the first priority in Figure 9 becomes active. Then the first driving signal is generated by Y₂ and X₃ in the word driving matrix. Therefore the first matching word is selected. After the first word clock is over, FX-3 is reset and the priority moves down to FX-8 enabling X₈. When the second word clock comes, the word driving signal is generated by Y₂ and X₈ in the word driving matrix to select the second matching words in the group 2. When the selection of all the matching words in the group 2 is finished, Y control reset Y₂ and enables next higher priority Y signal such as Y₁₁.

Now the states of matching signals m₈₁ through m₈₆ are stored in FX-1 through FX-8. Under the X priority control, the selection for the matching words of m₈₁ through m₈₆ will be performed. The selection process continues in the same manner under the X and Y priority controls until X-singlematch and Y-singlematch detectors detect end of the process. The logical diagram of Y-singlematch detector is shown in Figure 11. The X and Y-singlematch detectors are so designed to give a signal to the central processor for the preparation of the next action one word clock prior to the actual last word clock to speed up the interrogate repetition.

When the partial write operation is desired, the partial write control becomes active and in effect gives the function to by-pass the priority, therefore
CONCLUSIONS

The low-power requirements of the associative cell have made it possible to build an integrated MOS transistor associative memory system. MOS devices will be useful in large arrays of memory applications where fairly high-speed operation is required.

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REFERENCES


Four bits of associative memory on a single chip have been fabricated. However, it is expected to have a larger quantity of associative memory cells on a chip with MOS transistor circuits.

It is found that by decreasing the amplitude of interrogate drive pulses and increasing the mutual conductance of MOS transistors used for interrogation, the power dissipation in interrogate operation will be decreased and the signal-to-noise ratio on the word-sense line will be increased.

The method of multimatch resolving technique described in this paper is quite effective to realize a simple high-speed circuit system and an easy control of the partial write and single write operations.

Figure 11 – Logical diagram of Y-singlematch detector

X₁ through X₈ become simultaneously active depending on the states of FX-1 through FX-8.