INTRODUCTION

Macromodules are intended for assembly into a wide variety of computer structures with as few restraints on the designers' choice of the geometry of the machine as it is practical to require. The goal of geometric flexibility makes the problem of reliably interconnecting the modules to communicate data more difficult than usual. The ad-hoc repair of transmission failures is precluded because such problems would simple relocate as the system structure is altered by its users, and the detection and repair of the faults would be necessary after each alteration. Thus, as a practical consideration, hardware designs which do not eliminate such failures limit the system flexibility. Consequently, a substantial proportion of the engineering effort has focused on the data communication problem. Because the power distribution system interconnects the modules, it represents a set of pathways over which undesired signals may propagate. Therefore, power distribution has been considered in relation to the communication problem as well as in relation to its more direct effects on the design of the hardware. Because many details of the system and hardware design remain to be specified and because of the complexity of useful systems, no detailed noise calculations on such systems have been undertaken. Instead where a choice is permitted, the most conservative designs have been adopted with some restraints with respect to complexity. When the first small systems are complete, these early decisions will be re-evaluated, and, hopefully, at that point less conservative and simpler hardware will replace the present designs.

*A brief description of some typical characteristics of the modules helps in visualizing the design problems. As presently conceived, the macromodules will be selected from a set of 20 to 40 basic designs, and the bulk of the designs will range in logical complexity from as few as 50 to as many as 400 gate circuits. Current designs make use of emitter coupled integrated circuits having a typical rise time of six nanoseconds. It is anticipated that higher speed circuitry will be available in the near future and the hardware design is oriented toward the easy incorporation of this higher speed logic as it becomes available. The circuitry of a data gate module is shown in Figure 1 as a representative example of one of the smaller units.

Architecture

Two schemes of assembling the modules into a computing machine are under consideration. In the first scheme, the module cases mechanically interlock to form a rigid structure which is to be the whole of, or some portion of, the computer. The module case carries suitable sliding connectors which would permit adjacent modules to exchange digital information through the abutting sides. The front face of the module supports cable connectors through which information exchanged between non-adjacent modules travels, or for passing information between adjacent modules by means other than the sliding connector. Ground and power are distributed to the modules by a system of cables. A very simple system having these properties is shown in Figure 2. In the second scheme the modules are first mounted into a frame which has capacity for approximately 50 modules. The electrical paths provided by the sliding connector described above are replaced by a fixed array of wired interconnections between adjacent ports in
the frame. The front face of the module case supports a bank of connectors, and somewhat over half of the pins in the connector bank engage with connectors which are fixed to the frame and on which the wiring mentioned above terminates for the purpose of providing data paths between adjacent modules. The remaining pins on the module face engage the connectors of a “face plate.” This plate, one of which is associated with each module, carries the cable connectors which permit communication between non-
adjacent modules, and connects mechanically to the frame rather than to the module. Cabled data is funnelled back from the faceplate through pin connections between the module and the faceplate, into the module. The modules may be removed from the frame without disturbing the faceplate, and in this way the electronics may be removed without affecting the wired-in operational structure of the computer. An exploded figurative view of one frame section appears in Figure 3. Power and ground are distributed.
Data transmission problems

The electrical interconnections which carry digital information do so by carrying one of two d.c. levels separated by 0.8 volts. This low voltage swing together with a machine structure consisting of widely separated module assemblies cabled together and not enclosed in a single cabinet, suggest that unless unusual precautions are taken, noise will be a severe problem. The desirable mechanical flexibility conflicts with the compact, shielded type of structure which would be desirable from the point of view of noise. In the two modes of assembly described above, the noise problems differ only in detail. One may think of a frame holding modules as a module of increased complexity if, as is the case, the power and ground are distributed on a low impedance network.

Noise may be divided according to whether it is internally or externally generated. The externally generated noise is principally due to the electric and magnetic fields generated by equipment in the vicinity of the computer.

To attenuate the effects of external fields, a shielding system has been constructed around the computing machine, and this shielding reconfigures as the machine shape is changed. The shield system consists of the metallic module cases, and shielding which surrounds the signal leads, power cables, and ground cables. In the case of the frame supported system, the module case and the frame are electrically connected, so that the frame becomes part of the shielding. Where a lead or cable enter a module, the shield is terminated on the module case at the point of entry. The logic circuits are not grounded to their surrounding module cases. Thus, the shielding and cases form a low impedance path surrounding the whole system, but not electrically connected to it. It is anticipated that the shorted turns and low impedance paths to ground provided by the shielding will attenuate the noise generating effects of external electric and magnetic fields. The shielding of a small system is illustrated in Figure 6.

Among the sources of internal noise are the current and voltage transients which accompany a change in signal at some point inside the system. This effect may be reduced by transmitting signals over twisted-wire-pairs, shielded as described above, driven in a balanced mode. The twisted-wire-pair balanced mode couples very poorly with the surroundings. As a consequence, both the pickup and the radiation of noise in this mode are low. The integrated circuit logic provides, in many of the available gate packages, complementary outputs which are a suitable balanced signal source. If at the receiving end, one of the leads of the twisted-wire-pair is connected to the bias volt-
age input, the receiving circuit will behave as a differential amplifier. The sensitivity to balanced signals will be undiminished, but the ability to discriminate against unbalanced mode noise will be raised substantially. Since the unbalanced mode is reasonably well coupled to the surroundings, almost all noise appears in this mode. The above arrangement increases noise immunity in this mode from the 0.2 volts of the typical unbalanced arrangement to over 1.0 volt.

A typical signal transmitting channel is shown in Figure 5. The output stage consists of an emitter coupled integrated circuit gate with complementary outputs; a bifilar, 100 μh choke; a .01 μfd capacitor; and several resistors. This network serves three purposes: (1) it provides a terminating impedance (at the driving end); (2) it acts as a voltage divider for the output signal, and (3) it provides a high output impedance to unbalanced currents. The 1 K ohm resistors are provided to allow the output to swing negative when the emitter follower output is cut off. The detailed view of the output gate illustrates the need for these 1K ohm resistors. The choke is made by cementing two wires in parallel and winding the pair on a low Q ferrite core. Balanced currents will have cancelling fields and couple poorly to the core. Thus, the choke will represent a low impedance to these currents. The cancellation will not occur in the case of unbalanced currents. The choke will represent a high impedance to unbalanced currents and thus prevent their flowing out of the module to disturb the rest of the system. The output impedance of the integrated circuit is about 24Ω and forms a voltage divider when combined with the 130Ω, and 160Ω resistors. Although we have divided our driving voltage in half, the voltage differential at the receiving end is the same as in normal circuit usage. This is because the bias voltage input is not fixed as in the usual manner of use, but instead is driven oppositely to the signal input. The receiving gate acts as a differential amplifier. The unbalanced noise margin is increased by attenuating the balanced signal voltages as shown. The three resistors at the receiving end serve two purposes: (1) they bias the gate to a known state when the cable is not present; (2) they provide currents to cancel the 30 μa drawn by the more positive input terminal. Often, even though an input is unused, the user would like to know that the input is tied to a known level, and the bias network serves this purpose. The impedances of the biasing sources are sufficiently high so that the driving source and cable see virtually an open circuit when attached to the input. They are easily able to override the biasing network and apply the proper signal to the input. The biasing network is also designed to be unbalanced in such a way as to cancel the input currents mentioned above. This prevents the...
need to return those currents through the ground return.

Power distribution
A second source of noise that we classify as internal, although one might disagree with this classification, is the power line noise. Consider Figure 6. If the noise appearing at the transformer inputs is unbalanced in the sense that $V_{u1}$ and $V_{u2}$ are equal and in phase, then a current will circulate through the loop consisting of the transformers, the primary to secondary capacitances, and the grounding between the power supplies. Assume $C_1$ and $C_2$ equal $C_2$ and $C_4$ respectively. Then, if $V_{u1}$ and $V_{u2}$ are equal but out of phase, the problem is less serious and a sufficiently fast regulator response with a filter network having a sufficiently low pass characteristic will correct any problems. If $C_1$ and $C_2$ do not respectively equal $C_3$ and $C_4$, then even if $V_{u1}$ and $V_{u2}$ are equal and out of phase, current will flow in the ground reference. Power supplies that appear to be large enough to be useful imply a power transformer having substantial interwinding capacitances. In Figure 6 the reliability of signal transmission between the two logic modules at the top of the figure depends upon how much noise is present in the ground reference. In spite of the precautions of balanced signal transmission, an excess of current in the ground reference may generate a voltage drop exceeding the unbalanced noise immunity with the result that the receiving module may misinterpret the signal being transmitted. Thus, it would be desirable to keep the interwinding capacitances to a minimum and thus present the maximum impedance to power line noise generated currents.

There are several other considerations which enter into the specification of the power supply. Power consumption by the power supplies themselves can represent a substantial portion of the power dissipated in the computer. If the power supply is to be located near the modules, such as actually being attached to a section of frame, the total equipment power consumption in the vicinity of the operating modules will depend, in large part, on the supply's efficiency. The power consumption is very likely to be the factor which will limit the density of the system unless substantial liquid or forced air cooling is used. Because macromodules must be convenient to assemble, the additional complication of requiring cooling seems undesirable. In addition to efficiency, if the power supply is to be mounted in the frame, size and weight become important factors.

The preceding considerations lead to restrictions on transformer capacitance, power supply, size, weight, and efficiency. These restrictions suggest a supply in which the line voltage is rectified and filtered to give a high voltage at a low current and then converted, at a frequency which is high relative to the line frequency, to a low voltage at a high current. A block diagram of such a supply is shown in Figure 7. The conversion is achieved with the usual dc to dc converter and the efficiency is kept high by achieving line regulation of the output voltage with a pulse width regulator rather than a series regulator. The inverter transformer is small relative to a 60 cycle transformer and the capacitances assigned to it are also relatively small. Transformer droop and filter voltage drop which vary with load are compensated by a current feedback path.

Studies on a 20 amp, 5.2 volt supply indicate that the following performance goals are practical: (1) an efficiency somewhat exceeding 70%; (2) a weight less than 10 pounds; (3) a volume of about $3\frac{1}{2}'' \times 4\frac{1}{2}'' \times 8''$; and (4) less than 50 picofarads primary to secondary transformer capacitance.

A supply having these characteristics would be used in parallel with three others to power the units in a frame. An alternative approach would involve a single, larger supply designed to provide power to one frame.
section. In the method of assembly in which units are not mounted in a frame, but instead interlock as described earlier, the power supply design is less restricted and has not been considered in detail.

Construction details

The macromodule itself will consist of a metal case which surrounds several printed circuit boards to which integrated circuits are soldered. The board design allows 0.3 inch² of board per can. A typical case size is 3" × 5" × 10" with a board size of 4" × 8".

The printed circuit boards consist of four layers of circuitry separated by epoxy fiberglass as shown in Figure 8. The upper two layers provide signal interconnections between the integrated circuit cans. These two layers are separated by .006 inches of epoxy fiberglass insulation, and are in turn separated from the third layer by .032 inches of insulation. The third layer provides a ground plane which acts to confine the electric and magnetic fields of the interconnecting leads to the region between the lead and the ground plane. The coupling both between the leads themselves and between the leads and external electrical fields will be appreciably reduced by the presence of the ground plane. The fourth layer is an interdigital pattern which carries power and bias voltage to the circuit cans. It is separated by only .006 inches from the ground plane, and its capacitance to the ground plane provides some additional filtering of these d.c. voltages.

The clearance hole method of making connections between the can leads and interior layers, and between leads of the two circuitry layers has been chosen; manufacturing simplicity was the main factor in this choice.

Figure 8 – An exploded view of a multilayer board