INTRODUCTION

Techniques have recently been developed for using uncased integrated circuits in electronic systems. The use of uncased integrated circuits in computers will lead to the development of more reliable, more economical, and physically smaller computers than can be fabricated from discrete components or packaged integrated circuits. Before these advantages can be realized, practical techniques must be developed in the following areas:

1. Memory design
2. Logic design
3. Chip testing
4. Chip bonding
5. Chip passivation

All these areas are under study, and the initial results are promising. UNIVAC has been concentrating on developing techniques for achieving practical memory design, logic design, chip testing, and chip bonding. Several integrated circuit manufacturers are studying techniques for chip passivation, and economical processes should be developed within a few years. The design and fabrication of an integrated circuit, thin magnetic film memory system is described in this paper.

In addition to using uncased integrated circuits, the memory to be described also makes use of evaporated wiring and insulating layers. When fast rise times are required, the usual requirement of hundreds of milliamperes of drive current for operating magnetic memory elements is difficult to achieve with integrated circuits. The current requirements can be reduced by decreasing wire size to obtain a larger magnetic field per ampere or by using a storage element which operates with smaller magnetic fields. Both of these approaches are used in the memory to be described. The wire size is reduced to the point where evaporated conductors and insulators must be used to obtain tight coupling between storage element and wires. The use of evaporated wiring has other advantages which include compatibility with uncased integrated circuits and excellent reproducibility.

The memory system design is described in the next section. Emphasis is placed on the electrical characteristics of the system. The advanced fabrication techniques are described in the following sec-
tion. Production vacuum evaporation equipment and the chip testing and bonding process are also described. The physical layout of the memory and fabrication steps are given in the next to the last section, and the results are discussed and conclusions presented in the final section.

MEMORY SYSTEM DESIGN

The memory element configuration is shown in Fig. 1. The element is a thin film of electroplated magnetic material and is wired in a conventional manner with bit, dummy bit, and sense and cancellation lines. The word lines are 0.005 inch wide and are located less than 0.0005 inch from the magnetic element; drive fields of about 100 oersteds per emu are produced by the word drive currents. The memory operates with word drive fields of about 5 oersteds, and, consequently, requires only 50 milliamperes of word current. Bit and sense lines are 0.004 inch wide, and the memory requires only 20 milliamperes of bit current. The magnetic film is 800 angstroms thick and has an anisotropy field ($H_k$) of 1.5 oersteds and coercivity ($H_c$) of 2.0 oersteds.

The memory system consists of a 64-word, 24-bit-per-word rectangular array of storage elements, octal decoders, address registers, a selection matrix, word drivers, sense amplifiers, data registers, and bit drivers. All of these units are mounted on a common substrate. The circuits are all integrated and mounted (unpacked) facedown onto the evaporated aluminum wiring on the substrate.

The memory element output is about 1 millivolt in amplitude and 5 nanoseconds in width at the base. Output from the data register is at standard logic levels, and power dissipation is about 4 watts.

The memory system circuitry is contained on 178 integrated circuit chips. There are 10 different chip types of which 2 are of standard and 8 of custom design.

The word address and driver circuitry is shown in Fig. 2. The address register consists of 6 Motorola MC 302 flip-flops, and octal decoder A consists of 8 Motorola MC 306 3-input gates. The remaining circuitry is custom designed and is divided into the three chip types illustrated in Fig. 3. All of the PNP devices are grouped on a single chip so that the best characteristics of both NPN and PNP devices can be realized. Octal decoder B consists of 8 of the PNP chips, and the 64 matrix transistors are contained on 16-word switch chips. Word current pulses with a 50-milliamper amplitude and a rise time of less than 3 nanoseconds are generated by this circuitry. The amplitude of sneak currents in unselected lines is less than one milliamper.

A block diagram of the recirculation loop is shown in Fig. 4. The differential amplifier is designed for low noise and low power operation. The amplifier pulse gain is 12, its rise time is 3 nanoseconds and its common mode rejection ratio is 320. The amplifier stages are capacitor-coupled, and the coupling capacitors are included on the single-ended amplifier chips. The design shown in Fig. 4 makes it possible to use identical chips for the two single-ended stages. The pulse gain of the 2 cascaded single-ended stages is adjustable from 100 to 200, and the rise time is 3.5 nanoseconds. A strobe circuit which is used to gate the amplifier off except during the read cycle is on a separate chip. The data register is a standard Motorola MC 302 flip-flop. The bit driver circuitry requires both NPN and PNP devices. The integrated bit driver is fabricated on two chips, one containing all NPN devices and the other all PNP devices. The chips are designed so that one NPN chip and one PNP chip connected together form two bit drivers.

A typical chip is shown in Fig. 5. This is the single-ended amplifier chip, and the coupling capacitors can be clearly seen. All chips are
Figure 2. Word address and driver circuitry.

Figure 3. Word driver and selection matrix.
0.050-by-0.050-by-0.006 inch in size and are glass passivated for environmental protection. Critical circuits contain custom designed transistors. Use is made of evaporated nichrome for close tolerance resistors.

ADVANCED MANUFACTURING TECHNIQUES

The most serious problem resulting from the elimination of the integrated circuit package is that of providing environmental protection for the chip. The commonly employed passivation technique is to grow a silicon dioxide layer on the surface; this passivation coating has proved inadequate in environmental and life tests. Other techniques, which include the use of thin layers of low-temperature glass, thick layers of high-temperature glass, epoxy encapsulation, and silicone rubber encapsulation, have been tried with encouraging degrees of success. A satisfactory passivation technique will probably become available within a few years.

Other problems encountered with uncased chips are handling, testing, and bonding. A number of micromanipulators with vacuum pick-up devices are commercially available and provide adequate handling facilities. The problem of testing the chips is under study at UNIVAC. Chips are usually tested before wafers are diced or after they are packaged. Since the uncased chips are never packaged, only the wafer probing techniques are applicable to chips. Wafers are usually probed with long, needle-point, metal probes attached to small manipulators. These probes damage the probed area and are awkward to manipulate. More seriously, the size and shape of the probe make high-frequency testing of the chips impossible due to the inductance of the probe leads.

A high-frequency chip testing device has been developed at UNIVAC. A schematic drawing of this test equipment is shown in Fig. 6. The chip to be tested is held by a vacuum pick-up and positioned on a test card. The test card has a set of pedestals which correspond to the pad locations on the chip. The test circuitry is located adjacent to the pedestals on the test card, and no long, high-inductance leads are required. Consequently, high-frequency testing of the chip as well as low-frequency testing, is possible. A photograph of the chip test equipment is shown in Fig. 7.

The problem of bonding the chips to the circuit assembly has been solved by the development of an ultrasonic bonding technique. Pedestals are evaporated on the substrate at locations corresponding to the pad locations on the chip. Interconnect wires are evaporated onto the substrate to interconnect pedestals, memory elements, and external connec-
Figure 5. Single-ended amplifier chip layout.

The chip is located over the pedestals, and ultrasonic energy is applied. As many as 14 bonds are made simultaneously on a single chip. The apparatus used for performing the bonding operation is shown in Fig. 8, and a photograph of a bonded chip (viewed through the bottom of the transparent substrate) is shown in Fig. 9.

The problem of wiring substrates by evaporation appears formidable; however, practical production equipment has been developed. A typical 64-by-24 wired array of elements is shown in Fig. 10. This array has 3 layers of conductors and 3 layers of insulators and contains over 5,000 conductor crossovers. Units of this type have been produced in conventional vacuum system bell jars during a single pumpdown. Materials are evaporated through masks; masks, sources, and substrates are manipulated externally while the system is pumped down. Registration between masks is held to 0.0002 inch over a 1-by-2-inch substrate area. Although only a single pumpdown is required for completing the wiring of a memory system, production is limited to one or two per 8-hour day.

A production vacuum system has been developed for evaporating the conductors and insulators. An artist's sketch of the system is shown in Fig. 11, and a photograph of the prototype system is shown in Fig. 12. The input and output boxes contain substrate holders, each of which has a 13-unit capacity; these boxes are shown in Fig. 13. A trolley carries a substrate from the input chamber to the main chamber where all of the wiring is deposited in a sequence of evaporations through appropriate masks. The mask changer and operating mechanism
are shown in Fig. 14. When the evaporations are completed, the trolley carries the substrate to the output box and delivers a new substrate from the input chamber to the main chamber. When the substrate supply is exhausted, the input and output boxes are isolated from the system, new substrates are added, and completed substrates are removed. These boxes can be pumped down to operating pressure in 10 minutes. Consequently, the evaporation processes are not delayed for lack of substrates. The prototype system shown contains a single main chamber. This system can be easily expanded to include several main chambers. The following are some of the advantages multichamber systems provide:

1. Increased production by parallel operation.
2. Continuous production by sequentially isolating single chambers from the system for routine maintenance.
3. Provisions for performing low-vacuum and high-vacuum deposition techniques in different chambers.
The system shown can be used to produce 3 fully wired 6-by-3-inch memory planes per hour.

MEMORY SYSTEM FABRICATION

A plane view of the memory system is shown in Fig. 15. Word lines are on 0.020-inch centers, and bit and sense line pairs are on 0.060-inch centers. All lines are made of evaporated aluminum 20,000 angstroms thick; word lines are 0.005 inch wide, and bit lines are 0.004 inch wide. A cross section view through the plane is shown in Fig. 16.

The recirculation loops are equally divided on the left and right sides of the memory matrix. The entire word address circuitry and the word drivers are located at the top of the matrix. Two spring-type connectors provide all voltage and signal leads for the plane.

The fabrication steps for manufacturing the memory system are shown in Fig. 17. A glass substrate is covered with a copper ground plane formed by a combination of evaporation and electroplating steps. The copper serves as the conductor for electroplating the film of magnetic alloy, which is applied next. Following this step, the 64-by-24 array of storage elements is photetched, and the magnetic memory properties of the resulting elements are measured in a test setup which simulates memory operation. Planes with defective bits are rejected. After testing, the plane is installed in the production vacuum system where all the pedestals,
Figure 11. Artist's sketch of production vacuum system.

Figure 12. Production line vacuum system.

Figure 13. Substrate holder.
MAGNETIC THIN FILM INTEGRATED CIRCUIT MEMORY

Figure 14. Mask changer and operating mechanism.

wires, and insulating layers are sequentially deposited through appropriate masks. All wiring is completed in a single cycle through the vacuum system, and no etching steps are required. The wiring on the planes is next tested for continuity, shorts, and resistance. The pretested integrated chips are attached to complete the system. The memory is then given an operational test, encapsulated, and finally retested.

DISCUSSION AND CONCLUSIONS

The memory described does not represent the best that can be produced by the new techniques developed, but it does establish the applicability of the techniques to the fabrication of thin film memory systems.

The system could be made denser. The bit spacing and chip spacing were set by energy dissipation considerations. The bit spacing in the array shown in Fig. 10 was 0.030 inch; the 0.060-inch spacing was used in the final model so that the recirculation loop circuit chips could be spread over a larger area without fanning out. If the chips are spaced as shown in Fig. 15, temperature rise during operation is limited to a practical value. When the energy dissipation problem is solved, the chips can be placed as close as 0.010 inch apart by using the fabrication techniques already developed.

The system capacity is adequate only for scratch-pad applications. Larger systems can be made, but there is a limit to the length of line that can be vacuum evaporated through masks. A practical upper limit is presently considered to be 6 by 6 inches. When the energy dissipation problem is solved, 138,000 bits, including circuitry, could be placed on the substrate. This is still not adequate for large systems; however, larger systems could be fabricated by stacking planes.

The cost per bit of the memory system could be reduced by making higher-capacity planes. However, the most substantial decrease in cost will re-
Figure 15. Plane view of memory system.
result from reduced integrated circuit prices. The cost of integrated circuits has decreased substantially in the last year, and further reductions are anticipated. The use of uncased integrated chips should result in additional substantial reductions in the cost per circuit. The cost should reach such a low level that minimizing circuitry will not be a significant system design criterion. A parallel situation existed when integrated circuits were introduced with the result that transistors became less expensive than resistors. The estimated cost of 4,096-word memories of the type described is $0.02 per bit based on a $2.00-per-chip price. Since chip prices eventually fall below $1.00 per chip, memory systems costing less than $0.01 per bit are anticipated.

The reduced chip price and the fabrication techniques described may lead to a new concept in memories. Memories are presently formed by interconnecting components, such as storage arrays, word drivers and sense amplifiers. Rugged, compact, and inexpensive memory modules containing all the system circuitry may be made available in standard sizes for use as computer system components. This advance, which is potentially as significant as was the introduction of integrated circuits, which changed the component unit from the resistor, capacitor, and transistor to the entire circuit, could substantially alter the present concept of computer design.

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Considering all sources of delay, a memory cycle of 100 to 150 nanoseconds is easily obtainable in a memory consisting of a few thousand 32-bit words.

CONCLUSIONS

The experimental results have shown that the woven read-only memory array has the required properties for achieving very short memory cycle times. Another attractive feature of the memory is the high packing density which can be achieved; the results quoted on area packing density indicate that over 50,000 bits per cubic inch are obtainable.

The description of the fabrication method for the memory has shown that stacks can be assembled at very low cost per bit due to the highly automated nature of the memory production process. If the costs become as low as anticipated, it may even be possible to consider the woven memory array as a very high-speed semipermanent memory by using "throw-away" planes.

Finally, the results show that the memory element is insensitive to mechanical stresses and temperature changes. The woven array will therefore be applicable in those areas where highly reliable operation is required under extreme environmental conditions.

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REFERENCES