A FAST CONDITIONAL SUM ADDER USING CARRY BYPASS LOGIC

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INTRODUCTION

The higher speeds obtainable with present day logic circuits of various integrated circuit types increase the need for faster adders. The speed of addition can be increased primarily in two ways: (1) by more efficient logic organization, (2) by using faster logical elements.

Among the different binary full adders the best known perhaps is the iterated type or ripple carry adder.1,2 In this adder, the carry is propagated between adjacent ordered stages through relatively fast carry circuits, and the sum is generated after the carry propagation has been completed. It is recognized that in this type of adder the major portion of the required addition time is due to carry propagation time. There are several ways of speeding up carry propagation. Two of the most frequently used methods are the lookahead and the carry skip techniques.3,4,5 In each of these techniques the sum generation is subsequent to the speeded up carry propagation.

In the conditional sum adder, the generation of the sum is simultaneous with that of the carries. The conditional sum formation was first described by Sklansky in 19606 and later used by Bedrij in a parallel adder utilizing a parallel pyramidal type of logical organization.7 In the conditional sum adder described here the carry signal is propagated serially in two logically different paths. One of these paths is for the generation of the two possible carries of each binary stage and the other is to perform the carry bypass and selection logic. Because of the serial propagation of signals, fast circuitry is required.

The fastest available digital circuits today still use tunnel diodes and are fabricated by hybrid integrated circuit methods. Speeds of about an order of magnitude higher can be obtained with circuits incorporating tunnel diodes than with those using transistors only. The controversy about the future of the tunnel diode in digital computers stems from the fact that they do not lend themselves to the most promising type of integrated circuit technology, i.e., fabrication using monolithic techniques. In hybrid integrated circuits, however, the speed advantage of the tunnel diode can be efficiently exploited due to the decreased stray reactances of packaging and construction. Therefore, in this writer's opinion the future use of the tunnel diodes in digital computers will depend to a large extent on the acceptance of some sort of hybrid construction technology.

In the design of the adder, an approach useful for functional units appears to be the most suitable one and is the approach followed here.8 This design phi-
osophy makes use of the fact that optimization for the maximum performance per cost ratio is an easier task if the logic circuits have to perform only a pre-determined, limited number of logic functions. In this case a better coordination between logic and circuit design is also possible.

The logic organization presented here observes the capabilities and limitations of practical circuitry and topology. The circuit design conforms to the characteristics of the logic functions and takes into account the potential advantages of the microminiaturization techniques.

LOGICAL ORGANIZATION OF ADDER

The principle of the conditional sum adder is based on the computation of conditional sums and carries that result from all possible distribution of carries. Since for a binary full adder stage the carry can be either a one or a zero, only two conditional carries, and consequently two conditional sums, need be generated.

The illustration of the principle is shown in Fig. 1. Let us assume that two operands of \( N \) bits each are to be added. Both operands, and therefore the adder, are divided into \( k \) groups of \( n \) bits each (\( n \) does not necessarily have to be the same for every group). In each group the carry and a portion of the sum circuits are duplicated in order to generate the two carries and two sums corresponding to a possible one and zero carry input to the group. Having two sums available, a decision is then made as to which sum is the correct one and this in turn becomes the sum output.

The carry-bypass decision logic circuit determines the correct carries using the carry signals of the last stage of the group and the output of the previous bypass circuit. The decision logic is then propagated to higher order groups. The total worst-case carry propagation time for two operands of \( N \) bits is

\[
t_p = n_1 t_c + k t_g
\]  

where \( t_p \) is the total carry propagation time, \( t_c \) is the propagation time of the carry circuit within the group, \( n_1 \) is the number of carry stages in the first group, \( k \) is
the number of groups, and $t_a$ is the intergroup propagation time. This relationship assumes that the output signal of the last stage of a group is available by the time the decision signal reaches the corresponding decision stage.

The derivation of the decision logic either by the method of Karnaugh map or total induction is straightforward, thus only the end results are given here. The bypass decision function ($C_{Di}$) of the $i$th group of an $n$ bit grouping is as follows:

$$C_{Di} = C_{D(i-1)}C_{Yin} + C_{Nin}$$  

(2)

where $C_Y$ and $C_n$ are the carry output as shown in Fig. 1.

Unfortunately, the logical expression of Eq. (2) cannot be readily realized with one tunnel diode unit-delay. Also the AND circuit would require tighter component tolerances than required by an OR Circuit, thus contradicting the design goals. For these reasons, a different logic function whose generation is practical with a tunnel diode transistor circuit using the tunnel diode in the propagation path was needed. This circuit should have operation margins at least as good as a “one out of three” analog threshold circuit. By employing logic which is not of the minimal form, a convenient function was found, which is given in Eq. (3).

$$C_{Di} = C_{Yin} (C_{D(i-1)} + C_{Nin})$$  

(3)

This logic statement can be realized by an emitter coupled transistor-tunnel diode bypass circuit having the properties described above. More will be said about this circuit in the following section.

The sum is produced by two cascaded logical equivalence functions ($A \nabla B = AB + AB$) for both $S_y$ and $S_n$. The two sums are given in Eq. (4).

$$S_y = (A \nabla B) \nabla C_Y$$

$$S_n = (A \nabla B) \nabla C_n$$  

(4)

From this we can see that the first subsum can be combined for $S_y$ and $S_n$ and the circuit producing $A \nabla B$ does not have to be duplicated. Therefore, the expression for the sum of group $i$ stage $j$, including selection, is given in Eq. (5).

$$S_{ij} = (A_{ij} \nabla B_{ij}) \nabla [C_{Y(i-1)} \cdot C_{D(i-1)}$$

$$+ C_{S(i-1)} \cdot C_{D(i-1)}]$$  

(5)

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Figure 2. Block diagram of adder, eight groups — eight bits each.

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In order to eliminate the relatively slow logical equivalence circuits from the sum selection path the following logically identical expression was implemented in the actual adder.

\[ S_i = \left[ (A_i \lor B_i) \lor C_{N(i-1)} \right] \cdot C_{D(i-1)} + \left[ (A_i \lor B_i) \lor C_{N(i-1)} \right] \cdot C_{D(i-1)} \]  

The complete logical organization of the adder is given by the block diagram of Fig. 2. For reasons of speed and circuit simplicity, the input signals to the individual adder stages are the complements of the operand bits. Consequently, the complement of the carry rather than the carry is propagated. This way only the complements of the input signals are needed as inputs; greatly reducing packaging and interconnection problems. Each square on the diagram represents \( n \) adder stages in accordance with logical grouping and packaging. The \( C_n \) and \( C_y \) functions are generated by the carry circuits according to Eq. (8). Box \( P \) designates the decision logic circuit \( (C_n) \) and \( Q \) stands for the amplifier of the decision function for the selection of the proper sums. These are either \( S_{yi} \)'s or \( S_{ni} \)'s of Eq. (4). The iterative logical organization is clearly seen from the block diagram.

If we assume that each group contains the same number of stages, (this is a practical assumption for reasons of modularity and cost considerations, but does not give the highest obtainable speed), and that \( t_g = \alpha \cdot t_c \), then Eq. (1) becomes

\[ t_p = ntc + \frac{\alpha N \cdot tc}{n} \]  

where \( N \) is the number of operand bits.

If this expression is minimized as a function of \( n \), we obtain for the optimal number of stages within a group:

\[ n = \sqrt{\alpha N} \]

By taking \( \alpha = 1 \) (i.e., the intergroup stage delay is equal to the intragroup stage delay) we obtain:

\[ n = \sqrt{N} \]. For \( N = 64 \) this yields \( n = 8 \) and \( k = N/m = 8 \).

The timing diagram for a 64-bit adder is given in Fig. 3. The times shown represent worst-case design values with packaging and interconnection parameters taken into consideration.

![Figure 3. Timing diagram of 64-bit adder. A complete cycle is shown.](image)
CIRCUITS

The circuitry used in the conditional sum adder is designed to satisfy the constraint that the logic be built using not more than three different modular microcircuits. These circuits must be flexible enough to meet different requirements—either logical or gain—for the various applications. Each of these microcircuits is built on a separate ceramic substrate using hybrid microminiaturization techniques. Two of these circuits do not lend themselves to any other technique (unless the tunnel diodes are attached separately to monolithic circuits). The third circuit could be built with monolithic construction, however, at the time of the design the required speeds were not obtainable using the commercially available monolithic circuits. A snap-off diode pulse generator circuit was used for the generation of the clock pulses. This was built by miniature discrete components to be amenable to future modifications. However, in the construction of this circuit hybrid techniques could be used as well.

THE CARRY CIRCUIT

In order to obtain the required speed and simplicity in the adder logic, the complement of the carry signal rather than the carry is generated by the carry tunnel diode (Fig. 4). However, for the sake of easy reference, the circuit will be referred to as the carry circuit.

The Boolean equation for the complement of the carry function of the adder of jth binary order is given below:

\[ C_j = A_j B_j + A_j C_{j-1} + B_j C_{j-1} \]  

where \( A_j \) and \( B_j \) are the two operands of the jth stage; \( C_{j-1} \) is the carry function of the stage of the next lower binary order; \( C_j \) is the carry function of the jth stage. The barred symbols represent the complements of the logic variables defined above.

In the circuits of Fig. 4, the \( A_j \) and \( B_j \) signals are applied to terminals 7 and 8 respectively. \( C_{j-1} \) is applied to terminal 5. X and Y terminals are for the power supply voltages \( X = +6\,\text{V} \pm 1\% \), \( Y = +3\,\text{V} \pm 5\% \). The tunnel diode, \( TD \), performs "2 out of 2" analog threshold logic, i.e., the output of the tunnel diode is a one, if two or more of the inputs are ones; otherwise, it is zero. D-c bias is applied to the tunnel diode through the \( R_1 \) resistor, and conditional bias through the series resistor network of \( R_2 \) and \( R_3 \).

The tunnel diode is operated in the bistable mode using unconditional reset, with the reset pulse applied to terminal 6. Unilaterization between tunnel diodes is performed by a low peak current tunnel diode, \( B \). The carry function \( C_j \) appears at output terminal 10 and \( C_j \) appears at output terminal 9.

Figure 4. Circuit diagram of the carry circuit.

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THE BYPASS-DECISION CIRCUIT

The decision circuit, Fig. 5, is used for two functions: (1) to perform the carry bypass-decision logic and (2) to provide high-speed amplification. The circuit consists of two parts: (a) an emitter coupled transistor circuit and (b) a tunnel diode regenerative pulse amplifier or logical circuit.

When the circuit is used for the generation of the decision logic, the following logic function is performed: \( C_{Dk} = C_T (C_N + C_{Dk-1}) \). In this application terminal 5 is connected to terminal 6. Terminal

Figure 5. Decision-carry bypass circuit.

Figure 6. Characteristic curve and load lines of the tunnel diode.
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9 is connected to 8, and to 13 through a tunnel diode-resistor decoupling network shown in Fig. 5. The power supply voltages are $X = +6v \pm 1\%$; $Y = +3v \pm 5\%$; $Z = -6v \pm 5\%$. $C_y$ is applied to terminal 7; $C_N$ and $C_{Dk-1}$ are applied to terminal 10 and 11 respectively. The output is obtained at terminal 13. The tunnel diode characteristic with its load line is shown in Fig. 6. When $C_y$ is low (40 millivolts), the transistor on the righthand side conducts, and the tunnel diode is biased to point 1. There is not sufficient current to switch the tunnel diode even when $C_N$ and $C_{Dk-1}$ are both present. However, when $C_y$ is high (500 millivolts), the transistor on the righthand side is cut off and the tunnel diode is biased to point 2. Now, either of the two signals, $C_N$ or $C_{Dk-1}$, is capable of setting the tunnel diode to the high voltage state. The above logic function is thus generated. The tunnel diode is reset by an unconditional reset pulse through terminal 12.

In the second application, the tunnel diode is used as a buffer amplifier and the transistor circuit as a complementary current switching amplifier. Then terminal 8 is connected to terminal 9 and terminal 7 to 13. The input is applied to terminal 13 and the complementary outputs are obtained at terminals 6 and 8.

**Figure 7. Circuit diagram of gated logical equivalence circuit.**

**SUM CIRCUIT**

As described previously the sum function is generated by logical equivalence circuits. The sum substrate contains a NOR, a NAND, and an inverter circuit (Fig. 7). These circuits can be readily interconnected to provide the desired functions. In the first level of sum logic the inputs $A$ and $B$ are applied to terminals 5 and 6. Terminal 7 is connected to terminal 8. $X = +6v$; $Y = +3v$; and $Z = -6v$. The output $F = AB + AB$ is obtained at terminal 9. The operation of the circuit is straightforward, therefore only a short explanation is given here. When $A$ and $B$ are both low, neither $T1$ nor $T2$ conducts, therefore the output is high. When $A$ is low but $B$ is high, or vice versa, $T2$ is cut off but $T1$ conducts. Consequently, the output is low. When $A$ and $B$ are both high, $T2$ conducts making $T1$ cut off. As a result the output is high.

In the second level of sum logic, terminal 7 is connected to 8 and terminals 9, 10 and 12 are connected together. The input signals $AB$ and $C_D$ are applied to terminals 5, 6, and 13, respectively. $X$ and $Y$ are both connected to +6v and $Z$ to -6v. The output func-
tion \( F = (AB + AB)C_D \) appears at terminal 11. The operation of the circuit is the same as described for the first level circuit. In addition, the transistor amplifier circuit which is connected to terminal 9 manifests itself as an inverted AND output at terminals 9 and 10. The resistor diode network between terminals 12 and Z is part of a logical OR network required to obtain the sum output on a single terminal.

CONSTRUCTION AND PACKAGING

The circuit modules are fabricated on a 0.5 \( \times \) 0.75-inch alumina substrate. The photograph of the assembled substrate without the cover is shown in Fig. 8. The resistors and conductive paths are printed by silk-screening process. The transistors and rectifier diodes are of chip form and are mounted onto the substrate by high-compression bonding and solder flow techniques. The germanium tunnel diodes are encapsulated units in micro-epoxy packages. They are attached to the substrate by soldering. Fourteen pins of 20 mils in diameter are perpendicular to the substrate with center spacing of 125 mils. In the feasibility model, 4 adder stages are packaged on a 4 \( \times \) 4-inch mother board. A mother board contains 22 hybrid integrated circuits and a reset pulse generator, which generates a negative pulse of 5 nanoseconds duration and of \(-4.5\) volts amplitude. The board itself is a 5-layer board of 3/32-inch thickness using two layers of signal interconnections and a power supply plane between 2 ground planes as inner layers. The reset pulse is distributed via tapped, terminated transmission lines. The power distribution is accomplished by low-impedance transmission lines.

CONCLUSION

A complete adder motherboard was assembled and tested. Average stage delays of 0.3 nanoseconds and voltage margins better than \( \pm 8\% \) were obtained using tunnel diodes of \( I_P = 4.7 \text{ ma} \pm 3\% \) and minimum \( I_P/C \) ratio of 2.5 ma/pf. The high speed and good operating voltage margins are due to the isolation of the transistor capacitances from the tunnel diodes, the low stray capacitance construction and packaging techniques, and the large overdrive available for the tunnel diodes. From the experimental data obtained, the estimated add time of two 64-bit operands is 26 nanoseconds. This is approximately 20 percent faster than the maximal time of 32 nanoseconds. Due to its iterated logic organization, the adder is readily expansible. The add time of a 100-bit adder consisting of 10 modules of 10 stages is estimated to be approximately 30 nanoseconds.

With the exception of the tunnel diode, all other circuit elements can be fabricated by monolithic technology. However, since in both circuits the tunnel diodes are connected to input or output terminals, they can be attached separately to the monolithic circuits as part of the packaging procedure. With this approach, the speed of monolithic logic could be improved considerably where fast serial signal propagation is needed.
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REFERENCES


