IMPACT OF SCRATCHPADS IN DESIGN:
MULTIFUNCTIONAL SCRATCHPAD MEMORIES
IN THE BURROUGHS B8500

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The B8500 Modular Data Processing system is the latest design in the rapidly growing family of Burroughs Modular Computers. As in previous modular systems,1,2 the Burroughs Corporation has found it expedient and efficient to utilize scratchpad memories to enhance the performance of the computer and other modules. This paper will describe in detail the application of multifunctional scratchpad memories in the computer module of the B8500 system.

The overall system design of the Burroughs B8500 is described in a separate paper presented at this conference.3 It will suffice to review only the basic characteristics of the system as background for this paper.

The B8500 is an advanced design, high-performance modular data processing system. Three modules comprise the major building blocks of the system: the computer module, the input/output module, and the memory module.

COMPUTER MODULE

52-bit words: 48 data, 3 control and 1 parity bit
Push-down (Polish) stack of operands to help implement arithmetic operations
Absolute, indirect and five forms of relative addressing:
Base Index Register
Base Data Register
Base Program Register
Self Relative
Program Reference Table
Unlimited Index Registers
Binary arithmetic: 200-nanosecond addition (single precision integer)
Multiple multifunctional scratchpad thin film memories
Associative memory
Full repertoire of arithmetic, logical and character handling function
Memory protection registers

INPUT/OUTPUT MODULE

512 independent simplex channels
Multiple 52-bit words of thin film buffering per channel
One 104-bit descriptor word per channel

From the collection of the Computer History Museum (www.computerhistory.org)
Linked descriptors provide I/O processing with minimum computer intervention. Parallel byte transfers—variable from 1 bit to 51 bits. Maximum throughput of 590,000 bytes per second. Data transfer cycle time per byte (any size less than full word), 1.7 microseconds. On-demand servicing of input and output devices.

MEMORY MODULE

Thin film, destructive readout. 4096 words of 208 bits: each memory word contains 452-bit computer words. Cycle time 500 nanoseconds: access time 300 nanoseconds for 208-bit word. 16 module system capability:

- 65,536 — 208-bit words
- 262,144 — 52-bit words

Capability of executing lengthy memory-oriented descriptors independently of, and concurrently with, computer module processing.

Computer and I/O modules may total 16: at least one of each type must be included. Memory modules may be added up to 16 modules: (262,144 — 52-bit words)

The remainder of this paper will be confined to a discussion of the scratchpad memories that are part of the B8500 computer modules. The buffer memory of the I/O module could also be considered scratchpad, but due to the limitations of time and space, it will not be discussed.

INFLUENCE OF MEMORY MODULE DESIGN UPON SYSTEM

The B8500 memory module concept, with its efficient “four-fetch” organization, provides the rationale for much of the scratchpad utilization in the computer module. One memory address descriptor, transmitted to all memory modules along a common communications bus, will select the addressed module, and within that module will select one of 4096 208-bit words. This composite memory word, containing 4 computer words, data or instructions, is available for transmission to the computer module 300 nanoseconds after the arrival of the address. Stored in the read-write register, the 4 52-bit words are sequentially transferred (four-fetched) to the requesting module at the rate of one full parallel 52-bit word every 100 nanoseconds. Including transmission time of the address descriptors and the returning information, 4 52-bit words can be requested from a memory module and received at a computer module in a total of 1.0 microsecond, or an average of 250 nanoseconds per word. Similar speeds are available for writing; “four-store” is also possible in the B8500 memory modules.

This four-fetch, four-store capability influences to a great extent the use, size and organization of scratchpad memories for the B8500. In a gross sense, it may be stated that one of the uses of scratchpad is to buffer the four-fetches until they are needed, or, in the case of four-store, to buffer words of data until they are assembled into four-word blocks for transmission to a memory module for storage.

SCRATCHPAD CONCEPTS

At the risk of being pedantic, let us discuss for a moment the definition of scratchpad memories. Universally accepted definitions are difficult to find, but the following statement will represent the scratchpad concept to the majority of system designers:

Scratchpads are small uniform access memories, with access and cycle times matched to the clock of the logic, and which are closely coupled to the source and/or sink of the data.

This definition studiously avoids the inclusion of the functions to which the scratchpads are applied. It also does not mention the form of implementation. These variables are left to the ingenuity of the system and circuit designers. In the latter case, implementations may vary from discrete component flip-flop registers to thin film uniform access memories.

Historically, core memories were used as scratchpads in computers where the bulk memories were magnetic drums. In the case of the Burroughs D825 system, the scratchpad is thin film; the bulk memory is core. Implementation may eventually travel a full circle; with the advent of inexpensive integrated circuit flip-flop registers, the cost per bit of this implementation may become comparable with high-speed thin film memories.
SCRATCHPAD APPLICATIONS

Functionally, scratchpads have been used for a variety of purposes. A major application is the buffering of information flow among the main memory of computers, computational elements, and input/output elements. This use also provides a speed conversion between data source and sink. Look-ahead designs, in which block transfers of instructions and data minimize memory accesses and transfers, have used scratchpad memories.

A major utilization has been the storage of intermediate arithmetic or logical results from a computational unit, minimizing the time and program steps required to transfer information to main memory and retrieve it when later needed. An outstanding example of this application is the use of a thin film scratchpad for the "last-in, first-out" stack in the Burroughs D825.

Finally, in many cases, economy dictates the use of scratchpad memories. Many registers, formerly implemented with flip-flops, are now stored as words in scratchpad memories. Typically, such registers are utilized for index words, base registers, real-time clocks and similar relatively infrequent usages. While it is true that these registers could be stored in main memory, the lower access time of the scratchpad makes the information available more quickly and doesn't tie up main memory address logic and communications lines.

USE OF SCRATCHPAD MEMORIES IN THE B8500

Now to specifics: the use of scratchpad memories in the Burroughs B8500 computer module. Figure 1 represents a block diagram of the computer module. The major elements of the computer module are self-evident from the drawing but special attention should be given two blocks: the Local Thin Film Memories #1 and #2. These are two scratchpad memories; multifunctional in application, identical in physical construction and speed, different in word size and word length. Tied in with scratchpad #2 is a small 28-word associative memory (19 bits per word) whose use enhances the utilization of the scratchpad memory by providing content addressing as well as the conventional binary coded word addressing capability.

It must be emphasized that each of the two scratchpad memories contains its own independent addressing logic, sense amplifiers, and read/write registers. Each of the memories is available to the two processing elements of the computer module: the Arithmetic and Logic Unit, and the Address Arithmetic Unit.

The rationale behind the inclusion of local scratchpad memories in the B8500 computer module encompasses many of the reasons previously stated. Foremost among them, however, is the need for buffering of four-fetches of instructions and data in advance of their use, i.e., look-ahead. Also important are its uses as storage for intermediate results, as an economical implementation for registers and counters, and for the extension of the push-down stack.

The use of two scratchpad memories, rather than one common unit, is necessitated by the concurrency of operations in the computer module. Areas of each memory are assigned in a manner which permits simultaneous operations of the most frequently used functions. Ideally, it would be desirable to have a multiplicity of scratchpad memories; one for each function. Cost, space and power considerations prohibit such extravagance now. Future adaptations, to be discussed in later papers, may offer some hope in this direction.

SCRATCHPAD PERFORMANCE CHARACTERISTICS

The B8500 scratchpads are implemented by magnetic thin film techniques developed and organized into linear-select memory arrays at the Burroughs Defense and Space Group at Paoli. To realize the high-speed access requirement of 45 nanoseconds, the reading function is nondestructive, eliminating the need for a restoring write cycle when data are to be retained unchanged.

Insertion of new data into the local memories (writing) can be accomplished within the 100-nanosecond clock period of the computer module. For both read and write, the memory cycle time is 100 nanoseconds, permitting synchronous operation with the logic of the computer module operating at 10 megacycles per second clock rate.

Addressing of all words of each of the two memories is performed through explicit binary coded addresses, which may be generated by the subcommand control hardware or included in a field of data or instruction word. Twenty-eight of the 44
TO MEMORY MODULES

COMMUNICATION UNIT

LOCAL THIN FILM MEMORY #1
64 WORDS @ 52 BITS

LOCAL REGISTERS (24)

TEMPORARY DATA (8)

STACK EXTENSION (16)

LOCAL DATA BUFFER (66)

STACK REGISTERS (2)

ARITHMETIC AND LOGIC UNIT (48 BIT)

TUNNEL DIODE

ASSOCIATIVE MEMORY

28 WORDS @ 19 BITS

INSTRUCTION PROCESSOR

ADVAQ

SYLD

ADVAST

PCR

FINQ

FINST

DECODE

CONTROL SIGNALS

ADDRESS ARITHMETIC (21 BIT)

INTRAMODULE DATA BUSSES

LOCAL THIN FILM MEMORY #2
44 WORDS @ 72 BITS

INSTRUCTION LOOK AHEAD (16)

PROGRAM REFERENCE TABLE

AND INDEX WORDS (24)

STORAGE QUEUE (4)

words in scratchpad #2 can also be addressed by discrete output lines from the associative memory.

SCRATCHPAD CONFIGURATIONS

Scratchpad #1

Local Scratchpad Memory #1 contains 64 words of 52 bits each. This memory is utilized for four major functions:

1. Locally Used Registers and Counters
2. Temporary Data Storage
3. Stack Extension
4. Local Data Buffer

Registers and Counters. In this 24-word portion of #1 memory are stored a multiplicity of registers and counters that do not require frequent access by either the program or the hardware, yet which must be readily available within a clock cycle when addressed. Economy is the rationale in this
case; cost, power and space savings over flip-flop implementation are evident. Typical among the words stored in this memory area are: Interrupt Return Register, Base Interrupt Address Register, and Interval Timer.

Temporary Storage. This area is used to store literals and portions of multisyllable instructions. The latter usage stores syllables for the period of time from their detection and preliminary processing at the Advanced Station (ADVAST) until they are required at the Final Station (FINST). Eight 52-bit words are reserved for this function.

Stack Extension. Sixteen words in #1 scratchpad memory provide additional depth for the Polish stack above that available from the two hard stack registers associated with the arithmetic unit. Additional stack depth is automatically accomplished by automatic storing and fetching from the stack extension in #1 to an area in the memory modules; the depth of the stack is limited only by the total capacity of the memory and the permissible area assigned to it by the Executive and Scheduling Program (ESP). Four-fetch and four-store are used in stack transfers to minimize the traffic on the inter-module communication buses.

Local Data Buffer. This 16-word section of #1 is unspecialized scratchpad. The area is not reserved for a specific category of information but can be utilized under program control for storage of any data word or field. It is, however, the only scratchpad area that is capable of buffering four-fetch and four-store of data. Specific instructions are included in the machine repertoire to permit manipulation of data to and from the Local Data Buffer.

Scratchpad #2

Local thin film memory #2 possesses the same performance characteristics as #1 but contains 44 words of 72 bits each (Fig. 2). The additional word length is required so that it can be utilized with the associative memory; 52 bits hold a normal computer word, while the remaining 20 bits contain an absolute memory address to which it may eventually be sent for storage (two bits are control bits).

Three functional areas are contained within this memory:

1. Instruction Look-Ahead
2. Program Reference Table and Index Words
3. Storage Queue

Instruction Look-Ahead. Sixteen words of #2 scratchpad are used to store four-fetches of instruction words transmitted from the memory module in advance of their use in the instruction processing section of the computer module. This area, called Instruction Look-Ahead (ILA), can hold up to four such four-fetches of “packed” instructions. (Instruction words of 52 bits in the B8500 contain 1, 2, or 4 12-bit syllables.) Only 52 bits of the 72-bit words available are utilized in ILA.

Program Reference Table and Index Words. The 24 words in #2 scratchpad devoted to the storage of Program Reference Table (PRT) lines and index words utilize all 72 bits; 52 for the normal word and an additional 20 bits for the absolute memory address and 2 control bits. A word stored in this area can be addressed in either of two ways; by explicit addressing or by selection by an output of the associative memory. The PRT entries (copies of PRT lines in main memory) and index words are stored interchangeably within this 24-word area.

Index words provide an increment to an address accumulator to point to a specific memory location. Index words stored in #2 contain an index value, an increment and a limit field withing the first 48 bits. The PRT word may contain, within its first 48 bits, the starting address and an upper limit for a data area main memory.

The PRT word may also point to the starting address or the entry point of a procedure. (These are called Data Descriptors and Program Descriptors, respectively, in the B5500 nomenclature.) Appended to each type of word is an 18-bit field representing the absolute address in a memory module where it has been or will be stored.

When a word is inserted into this 24-word area a copy of its absolute address is placed in the 20-bit word field described above, and also into one of the 19-bit words of associative memory. As instruction steps are decoded in the instruction proc-
essor, those instructions calling for an index word or a PRT reference send the calculated fetch address (absolute address) both to the communications unit and to the comparison register of the associative memory. If the associative memory contains the identical address, a word drive line from the associative memory will read out the proper word in the related 24-word portion of #2 memory. The selected word (and its 18-bit address) will be read out nondestructively, and the request to the communications unit is canceled. Such a sequence takes only 100 nanoseconds compared with the 600 nanoseconds (minimum) required if the words were to be fetched from a memory module, or an even longer time if the 24 words were searched and compared sequentially.

The 18-bit address field of the 72-bit #2 memory is required when the words referenced by the associative memory must be returned to a memory module. The associative memory used in the B8500 cannot have its contents read out like a conventional memory. When the logic requires storing of an Index or a PRT word in main memory following its access from #2, the 18-bit field is used to provide the communications unit an absolute address for the store function.

Storage Queue. The 4-word portion of the #2 designated for use by the storage queue is similar to the Index and PRT area. In both cases 72 bits are used and reference is achieved either by explicit addressing or by selection via the associative memory. The storage queue contains words destined for storage and their absolute address. Since the storage function has the lowest priority in the communications unit, words are retained in this area until service time is available. In a manner identical to that described for the Index and PRT area, data being fetched are checked against the contents of the storage queue by the use of the associative memory.

This use is not included primarily to save time (although it does) but, more importantly, to ensure that the “newest” data are fetched to the computer. Fetching of data from a main memory location about to be updated by a word awaiting service in the storage queue would provide incorrect information to the program.

SUMMARY

This paper has presented an example of the application of scratchpads to the computer module of a large processing system. The utilization of multifunctional scratchpad memories in the Burroughs B8500 system has enhanced the performance of the system and has resulted in significant savings of space, power and hardware.

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REFERENCES