AN EXPERIMENTAL 65-NANOSECOND THIN FILM SCRATCHPAD MEMORY SYSTEM

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INTRODUCTION

As computers become larger and more complex, the need for a high-speed scratchpad type memory becomes greater. Furthermore, the size and speed requirements increase. An early memory, suitable for use as a scratchpad, was described by H. Amemiya, R. L. Pryor, and T. R. Mayhew.1 This memory used two ferrite cores per bit and had a read/regenerate cycle time of 200 nanoseconds. More recently, a 64-word by 20-bit thin magnetic film memory was described by G. J. Ammon and C. Neitzert.2 This memory had a read/regenerate cycle time of 125 nanoseconds and its speed was limited primarily by the electronic circuitry. A number of other memories and memory designs, suitable for use as scratchpads, have been reported in the literature.3,4,5 Future need for a 256 to 1,024 word memory having a cycle time of 50 nanoseconds has been indicated. A project was therefore initiated to study the feasibility of such a system.

At their present state of development, ferrite cores do not appear capable of such speeds. Thin magnetic film memories, on the other hand, are believed to be capable of this speed using transistor circuitry, provided the best circuit and packaging techniques are used. The goal for the project was therefore set as a 256-word by 25-bit thin film memory having a read/write cycle time of 50 nanoseconds.

MEMORY ARRAY

The memory array consists of two polished aluminum plates coated on one side with a 1000-angstrom continuous film of 80-17-3 NiFe Co. These are mounted back to back. A set of 128 word lines, etched from ½-oz copper backed with Mylar is placed over each film surface. The word lines are 10 mils wide and are on 20-mil centers and are grounded to a gold-plated portion of the film plate at the far end by means of a pressure contact. They have a characteristic impedance of 24 ohms and a delay of approximately 1.5 nanoseconds per line.

A set of digit and sense lines, also etched from ½-oz copper backed with Mylar, is placed over and orthogonal to the word lines. They extend completely around the two film plates and are spaced from the word lines by a sheet of 1½-mil Mylar. The digit and sense lines use an interdigitated arrangement in which the digit line consists of two parallel conductors 6.5 mils wide and 11.5 mils apart. The digit lines are driven at their center, from a 15-ohm line, and are terminated at their free ends with 27-ohm resistors. The resistors are trimmed to give a specified differential digit noise of not more than 2.5 millivolts, at the sense amplifier input, when the digit rise and fall times are 5 nanoseconds. The sense lines have a characteristic impedance of 54 ohms and are connected to their respective sense

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amplifiers by a pair of 50-ohm terminated coaxial cables. The ratio of signal to noise at read time is specified to be greater than 5 to 1.

SYSTEM ORGANIZATION AND PACKAGING

A block diagram of the system organization is shown in Fig. 1. The address is decoded in two steps. The second step consists of a word driver matrix with a driver for each word line and a 2-input AND gate at the input to each driver. The first step of decoding is provided by AND gates at the inputs of the matrix drivers.

A regeneration loop consists of a 4-stage sense amplifier, a gated flip-flop memory register and a bipolar digit driver. The polarity of the digit current is controlled by the information to be written and the location of the word being written. A timing circuit generates all timing pulses required for the system operation when initiated by a start pulse. Details of all circuits are given later.

All electronic circuits are packaged on small plug-in modules. Figure 2 shows a two-view photograph of a half digit driver.

It was decided that the feasibility of the system could be demonstrated if a minimum of 8 words and 6 bits could be operated at one time. Therefore, 6 regeneration loops and the associated portion of the timing circuit were constructed on one mother board. Top and bottom views of this board are shown in Figs. 3 and 4.

The complete system was mounted in an aluminum angle frame shown in Figs. 5 and 6. The bit board appears in the upper portion and the memory array in the lower portion of Fig. 5. Any 6 of the 25 digit and sense lines can be connected to the board by means of coaxial cables and connectors. The electronic circuits required for 8 words are mounted on a movable word board shown in the upper left hand portion of Fig. 6. All 256 word lines are brought out to connectors, visible in this figure, by means of miniature 15-ohm solid-wall coaxial cable, and any 8 lines can be connected to the word drivers by means of short pieces of 24-ohm flexible cable.

ELECTRONIC CIRCUITS

Except for the sense amplifiers and drivers, the electronics is based on a logic circuit shown in Fig. 7a. This circuit is very fast and can be adapted to perform a large number of functions in a very simple manner. This circuit performs the logical operations shown in Fig. 7b, but it can be varied to provide other numbers of AND-gate and OR-gate inputs. It can also provide the functions shown in Fig. 7c. By returning the direct output to one of the inputs, a set/reset flip-flop is obtained and its use as a one-shot multivibrator is explained later.

When driving a 70-ohm terminated line the output rise time is 3 nanoseconds and the circuit delay, at the 50 percent points, is 3 nanoseconds. Its speed can be increased slightly by the use of more recent transistors. The input impedance is roughly approximated by a resistance of 7,500 ohms in parallel with a capacitance of 5 picofarads. The output impedance appears to be 5.5 ohms but this value can be effectively decreased for large fanouts by splitting the load and using 2 or more output emitter followers. By employing 3 emitter follower outputs, a fanout of 24 has been obtained. In this case the rise and fall times were 8 nanoseconds and the circuit delay was 5 nanoseconds.

For the circuit shown in Fig. 7, the normal logic levels are +0.2 and +1.0 volts at both the input.
Figure 2. Front and back views of a plug-in module.
and output. It is shown later how these can be changed at the output when special loads must be driven.

*Timing Circuit*

A logic diagram of the timing circuits is shown in Fig. 8. These circuits are made from delay lines and variations of the basic logic circuit shown in Fig. 7. The timing unit receives a high level on the read/write input during a read cycle and a low level during a write cycle. The start and inverted start pulses are received simultaneously. The inverted start pulse is used to reset the memory register. The start pulse sets the word TP flip-flop at the top of the figure. This starts the word pulse and latches the address register. The start pulse is then inverted and delayed to end the word pulse and un latch the address register. A small delay is inserted in one of the latch lines to prevent a race condition in the address register.

The start pulse is also delayed and split into its direct and inverted forms. These are combined with the read/write level to give either a set pulse or a strobe pulse. During a write cycle the inverted start pulse is ANDed with the low read/write level to give a set pulse while during a read cycle the direct start pulse is ANDed with the high read/write level to trigger a one-shot multivibrator which in turn generates the strobe pulse. The one shot consists of a flip-flop in which the inverted output is delayed and returned to an input to reset the flip-flop and terminate the pulse.

The direct start pulse is further delayed and used to trigger another one-shot multivibrator which generates the digit timing pulse.

*Address Register*

The logic diagram of one bit of the address register is shown in Fig. 9. Circuit details and parameter values are shown in Fig. 7. When input a is high and input b is low the register is latched, and changes in the level of input c do not change the state of the flip-flop. This is the case for the duration of the word current timing pulse. When the
word pulse ends the address is no longer needed and input \( a \) goes low and input \( b \) goes high. The state of the flip-flop is then under the direct control of input \( c \). If \( c \) is high the flip-flop is set, and if \( c \) is low it is reset. Thus, an address is held in the register only as long as it is needed after which the register is free to accept a new address if it becomes available before the end of the cycle.

Matrix Drivers

The elements of the word matrix, which are individual word-line drivers, require input levels of \( +0.2 \) and \( +2.5 \) volts in order to give fast turn-on and turn-off. In order to supply these levels, a slight modification of the basic logic circuit, as shown in the schematic circuit diagram of Fig. 10, is required.

Word-Line Drivers

In order to attain a minimum sense voltage of 1.5 millivolts, it was predicted that a word current 0.5 ampere with a rise time of 6 nanoseconds would be required. The total delay of a word line and its connecting cable is 3.2 nanoseconds so that with a rise time of 6 nanoseconds the condition for the line to act like an inductance \( (t_r > 2t_d) \) is poorly satisfied. However, this condition was assumed in the driver design and the resulting schematic circuit diagram is shown in Fig. 11. Two drivers are packaged in one module.

The inductance of the word line and its connecting cable is approximately 65 nanohenrys and the supply voltage is limited to about 15 volts by the transistor breakdown voltage. If the transistor is an ideal switch and capacitor \( C \) is selected to give critical damping on the word current turn-on, the time required to rise 0.45 ampere is 3.6 nanoseconds. However, the turn-on time of the transistor increases this to more than 6 nanoseconds. As a result the capacitance must be increased beyond the critical value and the circuit becomes oscillatory. The computed value of \( C \) for critical damping is 18
Figure 5. Bit side of complete memory system less timing and connecting cables.

The value used was determined experimentally.

The fall time of the current is determined by the line inductance and resistor \( R \). If the diode has a zero threshold voltage and zero resistance, the computed time for the current to fall to 0.05 ampere is 6.7 nanoseconds. This fall time has an effect upon domain wall creep in the magnetic film and will be discussed later.

The first two transistors of Fig. 11 serve as an AND gate and the third drives the transformer. The 150-picofarad speed-up capacitor, in the emitter circuit of the third transistor, gives a large initial transformer voltage to turn the output transistor on fast. The field discharge of the transformer gives a large reverse base voltage to turn it off. The transformer also provides a d-c level shift making it convenient to ground the far end of the word line. The \( RC \) circuit between the power supply and the collector of the output transistor is made common to all 8 drivers. This reduces the space required for resistors and is permissible since only one driver is used at a time.

**Sense Amplifiers**

Figure 12 shows the schematic circuit diagram of a sense amplifier. Capacitance coupling is required between stages to eliminate drift in the d-c levels due to temperature changes. Each amplifier is packaged in two modules with the coupling capacitors connected between modules. One side of the output drives the sense input to the information register and the other side provides an inverted output for test purposes.

This amplifier gives a single-ended output of 1 volt for a differential input of 2.4 millivolt. With a very fast rising input, the delay through the amplifier is 5.6 nanoseconds, and the output rises in 4 nanoseconds. When a common mode pulse—having
an amplitude of 250 millivolts, rise and fall times of 4 nanoseconds, and a base width of 10 nanoseconds—is applied to the input the common mode output is not measurable. However, the unbalance in the amplifier produces a single-ended output of up to 1.9 volts, and the time required for amplifier recovery is about 25 nanoseconds. Waveforms under operating conditions are given later.

Memory Register

Each bit of the information register consists of a flip-flop made from one logic module as shown in Fig. 13. The schematic circuit diagram is the same as that shown in Fig. 7a except that a third AND gate is used and a feedback connection is provided to form a flip-flop. Strobing of the sense signal is unusual in that it is performed at the register input rather than in the sense amplifier.

Digit Drivers

A hybrid diagram of a complete digit driver is shown in Fig. 14. It consists of a positive and a negative driver in separate modules with their outputs paralleled at the digit-cable inputs. The logic on the input is necessary because a ONE is written with a positive digit current on the top plate and a negative current on the bottom plate. A ZERO, of course, requires the opposite polarities. Transformer coupling to the output transistors permits the use of the same type high-speed transistor for each current polarity. In order to properly drive the transformers, the logic circuits supply a high voltage output similar to that shown in Fig. 10.

This driver delivers a 200-milliampere current pulse to the digit line cable with a rise time of 6 and a fall time of 4 nanoseconds. The delay be-
Figure 7. Basic logic circuit: (a) Schematic circuit diagram; (b) logic function performed by Fig. 7a; (c) other logic functions obtainable.

tween the leading edges of the input timing pulse and the output current pulse is 8 nanoseconds when measured between the 50 percent points.

EXPERIMENTAL RESULTS

Temperature Effects

The input and output of a sense amplifier were monitored while the ambient temperature was varied from -45°C to +60°C. The variation in delay through the amplifier was less than 0.5 nanosecond and the variation in gain was less than 5 percent.

In another test two inverters, a flip-flop connected as a one-shot, and a matrix driver were connected in a cascade to drive all four inputs of two word drivers simultaneously. The word driver outputs were connected to short-circuited cables to simulate word lines and their input voltage and output currents were monitored while the ambient temperature was varied from -45°C to +80°C. In the range from 0°C to 55°C the input pulse to the word driver increased in width by 2.5 nanoseconds and the output pulse width increased by 5.5 nanoseconds. No
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Figure 11. Schematic circuit diagram of a word driver.

Figure 12. Schematic circuit diagram of a sense amplifier.

Figure 13. Logic diagram of an information-register bit.

change in delay of the leading edge through the word driver could be detected for the full temperature range.

Cycle Time

Figure 15 shows selected waveforms taken while reading and regenerating a ONE at a repetition rate of 10 megacycles. In curve (d), the sense voltage is too small to observe and the noise shown is substantially all common mode. In curve (e), the sense voltage is the first negative pulse and the remainder is digit noise plus the rewrite sense voltage. Curves (a) and (c) show 60 nanoseconds from the beginning of the start pulse to the end of the digit current. Curve (e) shows that the amplifier recovers from the digit noise 65 nanoseconds after the beginning of the sense voltage. Finally, curves (a) and (f) show an access time of 30 nanoseconds. Fig. 16 shows the amplifier output with a higher repetition rate. In this case the circuit is arranged to write a ONE after reading a ZERO and to write a ZERO after reading a ONE. Two sense ONE signals appear as negative pulses at 2 and 8 divisions from the left and a sense ZERO appears as a positive pulse midway between the ONES.

Increased Number of Words

Although the memory plane has a total of 256 words, electronics was built for only 8. However, physical path lengths and loading, for a full set of electronics, were closely approximated except for the loads on the matrix drivers. In order to show the effect of a 16-by-16 word-driver matrix, a matrix bus was loaded with an additional capacitance of 200 picofarads in parallel with 300 ohms. There was no appreciable change in either the leading edge of the word current or the amplitude or timing of the amplified sense voltage. However, there was an appreciable increase in the fall time of the word current. As will be shown later, this is not objectionable.
Creep Tests

Adjacent-word disturb tests were made in all four corners of both plates and in the central portion of the top plate. The test consisted of writing alternate ONEs and ZEROs once in a word after having predisturbed the word by writing the opposite information 10 times. The word was then disturbed by writing the opposite information 25 million times in each adjacent word. Finally, the original word was read out and checked.

Initially, when every word was used with a word-current fall time of 4 nanoseconds, information was lost in a large number of bits. Improvements were made by using only odd numbered words and short circuiting unused word lines and by increasing the word-current fall time to the value shown in Fig. 15(b). Under these conditions a few bits failed in one corner of each plate. A total of 9 bits, distributed among 3 words, failed.* In every case the information lost was a ZERO. Apparently, loss of information was due to easy-axis skew in the magnetic film. The presence of skew is indicated by the difference in the amplitude of the ZERO and ONE signal in Fig. 16.

*It later developed that a partial short between two word lines caused part of the failures.
CONCLUSIONS

These experiments show the feasibility of a 256-word scratchpad memory with an access time of 30 nanoseconds. By using faster transistors, now available, this value should be reducible to 25 nanoseconds. The read/write cycle time, however, will still be limited by the amplifier recovery so that with the best transistors available it appears that 60 nanoseconds are required.

REFERENCES


