INTRODUCTION

The SCM COGITO-240 is an electronic desk calculator which makes use of one sonic (magneto-restrictive) delay line as its primary memory element. Some 480 bits of information are held in the delay line circulation pattern. These are represented in a Pulse-No Pulse code; the insertion of a pulse into, or its emergence from, the delay line at a particular moment indicates the value one for the corresponding information bit. The absence of that pulse represents the value zero. For a memory unit of this type it is convenient to recirculate information at a rate which is of the order of $10^6$ bits per second. Thus a convenient value for the delay time of the line, and for the time of one complete recirculation of the stored information, is about one-half millisecond.

In the development of the COGITO design it proved preferable to make use of a rate of handling of information, as for example in the performance of an arithmetic operation, which is substantially smaller than the 10 bits per second recirculation rate. One reason for this preference is as follows: The circulated information bits compose 120 “characters” of 4 bits each. (Most of these are decimal digits.) These form three “visible” registers called K (for “keyboard”), Q (“quotient”), and P (the double-length “product”) register. Associated with each of these is a storage register of equal capacity, which is not displayed. Many of the operations of the calculator involve the transfer of the content of one register to another; from one visible register to another or from a visible to a storage register or conversely. These operations are facilitated by increasing the time of handling of each bit, hence the time in which it is conveniently available for such exchange processes, to cover the period in which all possible exchange partners pass through the delay line circuitry. The use of precession in the COGITO memory was, in part, motivated by this facilitation of the transfer operations.

It proved possible to provide the COGITO memory with a precession pattern which divorces the rate of information handling in arithmetic processes from the bit transmission rate of the delay line, and thereby to permit choosing each of these rates to fit the convenience of its associated circuitry. It is the
The purpose of this report is to describe that precession pattern and also several simpler patterns which provide some, but not all, of the desired properties. Many details of the system chosen were motivated by unusual aspects of the COGITO design and are not likely to be of widespread interest. They are not discussed here.

**TIMING CHAIN SYNCHRONIZATION**

A series of flip-flops, the timing chain, serves to count the successive one-microsecond-long time intervals in which successive information bits are delivered to and received from the delay line. The timing chain is driven by a free-running oscillator, the “clock.”

If the delay line were to be used merely to recirculate without change the 480 bits of stored information, then the task of the timing chain would be merely that of subdividing one “memory cycle”; that is, the period of time required for one recirculation of the stored information. That is, in fact, the task of an early part of the timing chain which serves to distinguish one from another of approximately 480 “clock periods” into which a memory cycle is divided. By reason of the precession system a longer period of time, called a “machine cycle,” becomes significant. The later part of the COGITO timing chain serves to count the 60 memory cycles in each COGITO machine cycle.

In a delay line memory of this kind there arises a problem of synchronization; that is, of ensuring that information-bearing pulses emerge from the delay line in an accurately controlled phase relationship with the clock oscillation. A straightforward way of ensuring synchronization is to impose rigid control on the frequency of the oscillator and on the delay time of the line, and to adjust one or the other of these parameters so as to bring about the desired phase relationship. As a measure of the necessary rigidity of control it may be noted that in a machine like COGITO a long-term drift in either parameter of 0.1 percent would be intolerable.

Hindall has described a method of synchronization which obviates the need for rigid long-term stability of these parameters. He uses a delay time, and therefore also a memory cycle length, which is substantially longer than the time required for the insertion of the entire body of stored information into the delay line. In each memory cycle a “marker pulse” which is distinguishable (for example, by greater magnitude) from the information pulses is set into the line before the insertion of the stored information. After the entire block of stored information has been received from, and reinserted into, the delay line there occurs a “silent period” in which no further information is received from the line. During the silent period the clock oscillator is disabled; that is, its oscillation is suppressed. The emergence of the marker pulse from the delay line, somewhat later, marks the end of the silent period and brings about the release from inhibition of the clock oscillator. The timing of the succeeding activities is controlled by the now-enabled clock. These succeeding activities are: the insertion into the line of a new marker pulse, the receipt from and the reinsertion into the line of the pulses representing stored information, the disabling of the oscillator for the following silent period, etc.

COGITO makes use of a method of synchronization which is distinguished from that of Hindall in that the marker pulse does not differ from the information pulses in magnitude or the like. Rather it is recognized as the marker pulse by reason of its emergence from the delay line during a silent period. That is, the first pulse to emerge after the clock has been disabled is accepted as the marker pulse and terminates the period of inhibition of the clock oscillator.

The silent period provides a convenient reference point for the description of the memory cycle. In the following the term “memory cycle” will be used to refer to a period of time which begins in one, and ends in the next succeeding, silent period.

With either the Hindall or the COGITO method of synchronization the oscillator frequency and the delay time of the line may, without harm, drift gradually; the duration of the silent period will change continuously to accommodate these drifts. (It must not, of course, be allowed to shrink to zero.) The possibility of continuous change in the length of the silent period, consistent with the desired synchronization, arises from the suppression of oscillation of the clock. During the silent period all phase relations from the previous memory cycle, in which a marker pulse and the block of information pulses were inserted into the line, are forgotten. After the silent period the phase of oscillation of the clock is determined by the time of emergence of the marker pulse and is thus consonant with the times of emergence of the information pulses. Although these two methods of synchronization provide tolerance of
gradual changes in the two parameters discussed, a sudden change in either, that is, a substantial change occurring within one memory cycle, would still lead to malfunction. Fortunately, such sudden changes are much more easily prevented than are long-term drifts.

PRECESSION PATTERNS

In a simple recirculating memory using the CO-GITO synchronization the duration of the memory cycle is equal to the delay time of the line, together with its associated circuitry, since each pulse is reinserted into the line simultaneously with its emergence. The word "simultaneously" must not be interpreted very literally, since the time of traversal of the associated circuitry is substantial. More precisely: the recognition of an emerging pulse permits the introduction into the line of a pulse which is of well-standardized magnitude, duration, and phase with respect to the clock oscillator. Figure 1 shows the simple recirculation without precession of a marker pulse and a group of information pulses, with the emergence and reinsertion shown as "simultaneous" in this conventionalized sense.

![Figure 1. Recirculation without precession.](image)

One-half of the 480 bits of memory held in CO-GITO, called "V-bits," represent the numbers held in the 3 visible registers while the remaining 240 bits, called "S-bits," form the storage registers. One S-bit and the corresponding V-bit form a "bit-pair." It proves convenient to handle the two bits of a pair together, for the most part, and to make them available for manipulation over periods of time considerably longer than a few microseconds. A simple way in which that can be done is illustrated in Fig. 2. The information bits which emerge from the delay line in the first memory cycle are named

s1, v1, s2, v2, ..., s239, v239, s240, v240

in the order of their appearance following the marker pulse. The first two bits, s1 and v1, form one bit-pair; the following two another pair, etc. As the first two bits emerge they are captured in two flip-flops, S and V respectively, and are not simultaneously reinserted into the delay line. The following 478 bits are reinserted immediately upon emergence. Following the insertion of bit v240, the bit (s1) held in S is inserted, and after it the bit (v1) is inserted into the line from flip-flop V. Only then is the clock oscillator inhibited in order to begin a silent period. The marker pulse which emerged immediately before s1 was not reinserted immediately but was inserted only at the time of emergence of the second information bit, v1. In that way the introduction of a gap between the marker pulse and the first information bit is avoided. In the second memory cycle the information bits emerge in the sequence

s2, v2, s3, ..., v239, s240, v240, s1, v1

and the first two bits, s2 and v2, are captured in S and V and are held for later reinsertion in the same way as the first pair was earlier, etc. It will be seen that in each memory cycle the sequence of 240 bit-pairs is cyclically permuted and that after 240 memory cycles the original sequence has been restored.

Figure 2 has been drawn so as to emphasize another feature of this simple precession pattern: the duration of the memory cycle is greater by two clock periods than that shown in Fig. 1. It is also to be noted that the "early part" of the timing chain

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must now distinguish 482 rather than only 480 clock periods following the appearance of the marker pulse. Atypical activities occur in the first two and in the last two of these.

In the system of Fig. 2 each V-bit is held in flip-flop V throughout one memory cycle (perhaps excepting the silent period) and is available there for leisurely manipulation, and one S-bit is similarly held in S. After one machine cycle, consisting of 240 memory cycles, all information bits have thus been held and the original bit-configuration has been restored. It did not prove convenient to use in COGITO a machine cycle quite so long as 240 memory cycles (about one-eighth of a second) and therefore a slightly more complex precession pattern was considered.

A further classification of the information-bits held in the COGITO memory must now be described. Most of these bits represent the decimal digits which constitute numbers held in the various registers. Each decimal digit is represented by four bits, called $t_1$, $t_2$, $t_3$, $t_4$ in order of increasing significance. (A simple 1, 2, 4, 8, BCD representation is used.) It therefore proves convenient to organize all other information held—decimal point positions, plus or minus signs, etc.—in similar 4-bit characters. Thus the entire body of stored information may be divided into 4 equal parts; a group of 120 bits (60 bit-pairs) which are $t_1$-bits, 120 $t_2$-bits, etc. The transfers of numbers from one register to another respects this separation into four groups; in such a transfer a $t_1$-bit always remains a $t_1$-bit, etc. Thus it proves convenient to separate the body of stored information into four parts, and to introduce a precession within each part separately. Such a precession pattern is shown in Fig. 3.

To reflect the separation into four groups the 480 bits held in memory are renamed as follows. The 120 $t_1$-bits are called $s_1^{11}$, $v_1^{11}$, $s_1^{12}$, $v_1^{12}$, etc. In the first memory cycle (of a machine cycle) these 480 bits emerge from the delay line in the order named: the 120 $t_1$-bits follow immediately after the marker pulse, then the $t_2$-bits, etc. The first information bit, $s_1^{11}$, is copied into flip-flop S and is not immediately reinserted. Then the second bit, $v_1^{11}$, is copied into flip-flop V and a marker pulse is inserted into the line at this time. (It is the first pulse inserted since the silent period.) In the following 118 clock periods the remaining bits of the $t_1$-group are reinserted immediately upon emergence. Then, however, when the first bit of the second group, namely $s_1^{12}$, emerges from the line it is exchanged with the content of flip-flop S. That is, the emerging bit is set into flip-flop S while the prior content of S is returned to
the delay line. In the next clock period the content of flip-flop V, namely v1, is set into the line and the bit v1 is placed in flip-flop V. The remaining bits of the second group are then reinserted as they emerge. Similarly, the first two bits of the third group are exchanged with the contents of flip-flops S and V and the rest reinserted, and similarly during the emergence of the fourth group. After the emergence and reinsertion of the last bit of the fourth group (v60), the contents of flip-flop S and V are inserted into the delay line in two further clock periods in the same way as has been described for the simpler precession pattern of Fig. 2. The bits thus returned to the line are s41 and v1 respectively.

As can be seen in Fig. 3, the operations just described result in a cyclic permutation of the 60 bit-pairs of each group separately—together with a rightward displacement of the entire pattern in the same way as in Fig. 2. After one machine cycle, consisting of 60 memory cycles, the original configuration has been restored. During that machine cycle each V-bit has been held in flip-flop V, and each S-bit in S, for one-fourth of one memory cycle (with the neglect of the silent period).

In the discussion above attention has been directed to the circulation and precession of the bits of information held in storage in a delay line. The possibility that the value of an information-bit may have changed by reason of an inter-register, or an arithmetic operation, etc., has not been mentioned. Each of the symbols used, such as v1, should, however, be understood to represent merely the name of a variable which may change its value from time to time by reason of activities not described.

The precession pattern illustrated by Fig. 3 fails to provide one essential feature of COGITO. Each V-bit (that is, each bit of a “working register”) upon being picked up into flip-flop V must be provided with opportunity for leisurely interaction with the fourth bit to precede or succeed it in occupancy of flip-flop V (that is, the corresponding bit in another register, with which it may be involved in arithmetic manipulation.) For this reason a bit which has been held in V for a quarter of a memory cycle (called a “bit period”) is not, in fact, returned to the precession pattern as has just been described. Instead, it is set into a 4-flip-flop shift register in which it remains easily accessible for 4 additional bit periods, that is, for an additional one memory cycle. A bit which is held in storage in flip-flops in this way may be changed in value in any one of these 5 bit periods. After this holding period the (possibly modified) V-bit is returned to circulation as illustrated in Fig. 4. By reason of the general precession the time for rein-
Figure 4. COGITO precession pattern (shown for third memory cycle of a machine cycle). The information bits are shown as ambiguous, pulse present or absent.

sersion of the bit which has been held out of circulation for an additional memory cycle is immediately before, rather than after, the clock period in which the bit held in S is reinserted. In the clock period following the reinsertion of the S-bit no pulse is set into the line, thus the bit pattern shown in Fig. 4 has one-clock-period-long gaps there. The “bit value” shown with these gaps is zero. The omission of four bits from the pattern shown in Fig. 4, which is otherwise like that shown in Fig. 3, can be understood as arising from the fact that at each moment four bits are held out of circulation in the flip-flop shift register.

CONCLUSION

These examples illustrate the considerable flexibility of delay line storage systems provided with simple precession patterns. It seems likely that similar techniques will prove helpful in many situations in which the desired rate of handling of data is smaller than that convenient for a delay line memory.

REFERENCES