CIRCUITS FOR THE FX-1 COMPUTER
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Summary
A set of computer logic circuits capable of 50-megapulse operation is described. Included are gated and mixing pulse amplifiers, a static flip-flop, a diode logic unit with current-steering amplifier, a passive delay line, and an active variable delay circuit, all of which are designed to operate with terminated 75-ohm transmission lines. Ten-nanosecond pulses and 20-nanosecond flip-flop transition times are achieved through use of very-high-speed MADT transistors. The circuits have been successfully employed in the FX-1, a small general purpose computer with a high-speed magnetic-film memory.

I. Introduction

The FX-1 Computer is a small, high-speed, general-purpose digital computer designed and built, at the Massachusetts Institute of Technology, Lincoln Laboratory, to be a realistic test vehicle for high-speed logic circuits, packaging techniques, and magnetic-film memory.1

It is a parallel, binary, stored-program machine with a 12-bit word length (plus parity) and addressing capability for 1024 words. The present memory, however, contains 256 words plus a 16-word toggle switch storage for read-in and check-out programs. The transistor logic circuits operate at a 50-megapulse rate; that is, the contents of flip-flop registers may be interchanged or modified at 20-nanosecond intervals. The magnetic-film memory has a read-write cycle time of 350 nanoseconds. Approximately one-million single-address instructions can be performed per second. The instruction code is fairly small but provides relative and deferred addressing. The total number of transistors in the machine exclusive of memory is 3500.

Transistors

The logic circuits have been designed around a germanium p-n-p Microalloy Drift transistor, the L-5447, which was developed and brought into production early in 1960 by the Landsdale Division of Philco Corporation with support from Lincoln Laboratory. A later smaller version of this transistor is the T-2217, and commercial modifications are available as the 2N769 and 2N7975. The important characteristics of this transistor, as shown in Table I, are its high gain-bandwidth product and its low base resistance, collector capacitance, hole-storage, and saturation voltage. However, the gain-bandwidth product falls off above 10 ma. of collector current as shown in Fig. 1, thus limiting the class of usable circuits to those having relatively high load impedance.

In addition to the L-5447, a few 2N781 germanium epitaxial mesa and 2N708 silicon epitaxial mesa transistors were used where their higher current and dissipation capabilities were needed.

Design Constraints

At the desired speeds the transmission delay associated with just a few inches of wiring becomes comparable to the rise time of the signals. Terminated transmission lines are, therefore, indicated for most of the logic circuit interconnections in order to reduce crosstalk and reflections.

Since transmission line impedances are relatively low, the logic circuit is a transformer-coupled pulse amplifier so that the high load impedance needed for best performance from the transistor can be provided.2,3

II. Circuits

Gated Pulse Amplifier

The gated pulse amplifier, shown in Fig. 2, is somewhat unusual in that it has degeneration in the emitter circuit. Its operation can be demonstrated by considering the effect of a negative 1.7-volt step applied to the input (the base of Q1), assuming that the gating point (the collector of Q2) is grounded. The input voltage and the emitter resistor determine a maximum value for the collector current in Q1. This current is more than adequate to bring the transistor into saturation, thereby applying the supply voltage to the diode consisting of the collector RC network, the pulse transformer and its load, and the emitter RC network. However, the current in the magnetizing inductance of the transformer increases with time until eventually the available collector current is exceeded. The transistor then comes out of saturation and terminates the output pulse.

This circuit combines the advantages of saturated operation (the output is determined primarily by passive components) with the fast turn-off time of a nonsaturated circuit. If an output pulse from a similar circuit is applied to this circuit, the pulse is amplified and restandardized to a minus 1.7-volt peak amplitude and a 10-nanosecond width. Shorter than standard pulses are lengthened by hole storage while longer pulses are shortened by the shaping action described above.

The capacitor in the emitter circuit speeds-up the output rise time. The most important

*Operated with support from the U.S. Army, Navy, and Air Force.
function of the RC network in the collector is to reduce the collector supply voltage at the end of the pulse so that the peak collector voltage is reduced during the transformer overshoot. The collector RC network also causes some drop in the output pulse, although this has not been found objectionable. The overshoot voltage of the output pulse is determined by the magnetizing inductance of the transistor and the load resistance, which is always 37 ohms, hence no clamping is required to limit the back voltage on the transistor.

The design of the pulse transformer is crucial to the correct performance of this circuit. It is wound on a very small pair of Ferramic Q2 cup cores. The 14-turn primary and 3-turn bifilar secondary are wound over each other with the distributed capacitance and inductance carefully controlled in order to provide the proper characteristic impedance and resonant frequency. The secondary turns are lumped near the end of the primary which is ac grounded.

A special cable terminator is used at the input to the pulse amplifier to compensate for the capacitive, non-linear input impedance. A 100-ohm resistor can be used with some increase in rise time and delay.

Transistor Q2 of the gated pulse amplifier, Fig. 2, enables or disables the amplifier. If Q2 is saturated, the circuit operates as previously described; however, if the gate transistor is cut off, collector current will not flow in Q1 and an output pulse will not be produced. Stray capacitance at the gating point is charged to minus 1.1 volts when Q2 is cut off, in order to prevent a spurious output pulse. Since the pulse amplifier draws current from the gate transistor only when it is amplifying a pulse, Q2 may be used to enable or disable several amplifiers, provided the amplifiers are not pulsed simultaneously. Several gate transistors may be paralleled to obtain more complex gating logic. The gate transistor input, which is either at 0 or minus 1.5 volts, comes from a flip-flop or other level amplifier via a terminated 75-ohm transmission line. Up to 5 gate transistor inputs can be driven from a 75-ohm line.

Each pulse amplifier can drive two 75-ohm lines; if only one line is used, a 75-ohm padding resistor must be added. The output of a line may drive two pulse amplifiers if they are located within several inches of each other. Thus a fan-out of four is obtained with certain geometrical limitations.

The output pulse from the gated pulse amplifier has a minus 1.7-volt peak amplitude, 10-nanosecond width, 2-nanosecond rise time, 3.5-nanosecond fall time, and 1.3-volt overshoot. The circuit exhibits unity voltage gain for input pulses larger than minus 1.3 volts and has essentially no output for input pulses smaller than minus 0.5 volts. This provides good discrimination against spurious pulses and noise, and adequate margins with normal pulses.

The pulse propagation delay in this circuit is 3 nanoseconds of which nearly half occurs in the transformer. A change in the gate transistor input level must precede the input pulse by at least 10 nanoseconds to produce a proper output pulse. This "gate set-up time" is a function of stray capacitance at the transistor collector.

The maximum repetition rate for the pulse amplifier is limited to 25 megapulses per second by transformer recovery time. However, this limitation only rarely prevents the FX-1 from operating at an effective rate of 50-million register transfers per second.

Mixing Pulse Amplifier

A further extension of the basic pulse amplifier is shown in Fig. 3. In this circuit, the mixing pulse amplifier, transistor Q3 is added between the collector of the pulse input transistor and the pulse transformer in order to isolate the input transistor (now called a pulse inverter) from the large voltage swing at the transformer primary. Transistor Q3 operates as a grounded-base amplifier with a small amount of base degeneration. It saturates during the pulse and unsaturates at the end in a manner similar to that of the original pulse amplifier. The input signal to the mixing transistor is approximately 1.5 volts with a pulse current of 15 ma.; hence, the input impedance is 100 ohms. Several parallel pulse inverters may feed this low-impedance point, producing an output pulse whenever an input pulse is applied to any one of them. As is shown in Fig. 3, pulse inverters may be gated by gate transistors as in the case of the gated pulse amplifier. Because of the third transistor, the pulse delay time is increased to 4.5 nanoseconds; however in all other respects its characteristics are equivalent to those of the gated pulse amplifier.

Fig. 4 shows an input and output pulse for a mixing pulse amplifier. The slight ringing is due to the distributed capacitance of the transformer windings.

Flip-flop

The circuit schematic of the flip-flop is shown in Fig. 5. Transistors Q1 and Q4 are mixing pulse amplifiers similar to those previously discussed. The pulse transformers have been modified to provide secondary center taps. Transistors Q5 and Q7 form a conventional saturated NO-coupled flip-flop. Triggering is accomplished by driving both the "off" and "on" transistors to their new states by the input pulse. As a result the output transitions, as seen in Fig. 6, are very symmetrical. In addition, this triggering method improves the rise and fall times of the output since the capacitors in the cross-coupling arm of the flip-flop can be made smaller. These capacitors need only remove the stored charge from the 1N903 silicon mesfet diodes. Transistors Q5 and Q8 (2N761's) are output
emitter-followers, each capable of driving a single terminated 75-ohm line. Resistors placed in series with the bases of the emitter-followers prevent oscillation and ringing on the outputs. Standard output levels are 0 and minus 1.8 volts with rise and fall times of 5 to 8 nanoseconds. The note that the clamping voltages for the flip-flop are locally generated by the silicon diode net in the upper right corner. This has been done in all FX-1 packages in order to simplify power distribution. Transistors Q2 and Q3 provide steering for the complement input. These transistors are similar to mixing pulse amplifiers; however, their bases are biased from the outputs of the flip-flop. Therefore, an inverted pulse applied to their common emitters is steered either to the clearing or setting transformer. As seen in Fig. 6, the delays within the flip-flop, due to the transformers, diodes, etc., are greater than 10 nanoseconds, which is adequate to allow pulse dodging. The flip-flop can be used in shift registers or for register interchanges without auxiliary delay or storage. Each input terminal can be driven from up to 6 pulse inverters, with an input pulse arriving at one terminal or another at 20-nanosecond intervals. The pulse inverters may be conditioned by gate transistors as described in the pulse amplifier discussion. The transition times of the flip-flop are less than 20 nanoseconds.

Register Driver

The circuits previously described comprise the bulk of those in FX-1. Several others are required for the control and in-out sections of the machine. One of these is the register driver which is used to amplify command pulses for driving a flip-flop register. It consists of a grounded-base amplifier using an NPN silicon epitaxial mesa transistor and an output transformer. It will drive eight 75-ohm lines with an output pulse slightly wider and slower than that obtained from a standard pulse amplifier.

Timing Circuits

The control section of a computer requires circuits which can generate the chains of command pulses needed to perform instructions. In most computers, these command pulses are obtained from a clock, however, in FX-1 they are obtained from a large complex multipath delay-line loop. The exact path taken through the control is a function of the states of control flip-flops. Hence, a sequence of pulses in space and time is produced which is determined by the instruction to be performed. This type of control was used because it is more easily realized in a machine employing pulse logic circuits.

Delay Line

Two types of delay are used in generating the pulse sequences. One is a passive delay line, the other an active variable delay circuit. The passive delay line, shown in Fig. 7, is a folded strip-transmission line etched on one side of thin double-clad etched-wiring stock. By using a very thin dielectric, 0.01-inch thick Teflon, and narrow lines, a delay of 4 nanoseconds at 75-ohm impedance can be obtained in an area of approximately 2 square inches. Due to the fineness of the strip line there is a signal loss of 0.035 volts per nanosecond. Therefore, a special pulse amplifier was designed which produces a 60% larger pulse for driving the delay line. This pulse can traverse up to 40 nanoseconds of passive delay line before it is attenuated to the point that it needs amplification. Approximately 300 of these lines are used for spacing and trimming high-speed command pulses.

Variable-Delay Circuit

The active variable-delay circuit, shown in Fig. 8, is used for delays exceeding 45 nanoseconds, as for example, in memory-strobe timing, parity-check timing, and carry-propagation timing in the adder. Transistors Q1 and Q2 form a single-shot multivibrator which is triggered by the collector of Q2. The lower J1903 diode at the base of Q3 applies a positive step to the 82-m uf. timing capacitor. When the capacitor has charged, Q1 starts to conduct again, cutting off Q2. This same diode then opens allowing the pulse transformer to overshoot. This overshoot is amplified and standardized by the output pulse amplifier to produce the delayed pulse. Delays can be produced in the range from 45 to 160 nanoseconds; larger values require adding an external capacitor.

Diode Logic Circuit

When a large number of terms are to be combined into a single gating function, pulse logic is not desirable because the pulse must be passed sequentially through a pulse amplifier for each term involved, resulting in an excessively long logic delay. Level logic reduces the delay by producing the complex gating function for a single pulse amplifier. It is also superior for memory parity computation, where it permits the use of a pyramidal rather than a serial arrangement of gates.

The parity function of 4 bits can be obtained with a 3-level logic circuit, that is, an "and/or/and," if the inputs are available in both their normal and inverted forms. Normal and inverted gating functions are also necessary in delay-line-loop control logic, since a pulse is usually routed down either one or another of several delay paths. These requirements were met by using a 2-level diode-logic net followed by a current-steering amplifier which provides the third level of logic and the complementary output levels. The outputs of the current-steering amplifier are shifted with Zener diodes, clamped to locally generated voltages, and then amplified by emitter-followers so that terminated output lines can be driven. Several additional inputs were added to the diode net so that the unit

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would be more generally useful.

Fast silicon mesa diodes (1N903's) are used in the diode nets, L-5447 transistors in the current-steering amplifier, and 2N761 epitaxial mesa transistors as the emitter-followers. The delay time of this level logic circuit is 10 nanoseconds; the input and output levels are at 0 or minus 1.8 volts.

**Level Amplifier**

The level amplifier is an RC-coupled saturated L-5447 inverter driving a 2N761 emitter-follower, similar to half of the flip-flop of Fig. 5. It has a delay of 6 nanoseconds, and will drive one 75-ohm line with standard FX-1 levels having 3- to 6-nanosecond rise and fall times.

**Schmidt Trigger**

The Schmidt trigger circuit, Fig. 9, is used to amplify and sharpen slowly changing signals coming from switches, push buttons, or the lower speed logic circuits of the in-out equipment. Its output is a standard FX-1 level which can, if desired, be applied to a special pulse amplifier to produce a standard FX-1 pulse on the negative transition of the input signal.

### III. Construction

A three-level method of construction is used in FX-1. Circuit components are wired into small plug-in-units which plug onto trays. These trays contain most of the logic interconnections and are in turn plugged into boxes which contain the intertray wiring. This 3-level arrangement reduces the size of the machine and the wiring delays, without limiting accessibility.

**Plug-In-Units**

The circuit components are assembled in a cordwood fashion between two double-sided etched-wiring cards with plated-thru holes to form the plug-in unit, Fig. 10. Each unit, which measures 1 3/4" x 2 1/4" x 1", contains approximately 60 components and 10 transistors, which corresponds to one flip-flop or four gated pulse amplifiers. Small commercially available components are used, including 1% molded deposited carbon resistors and miniature ceramic capacitors. The assembly of the cordwood units proved to be quite simple and, contrary to expectations, repair has also been easy. Approximately 360 plug-in-units of 13 different types were used in FX-1.

**Trays**

The tray, shown in Fig. 11, will mount and interconnect up to 20 plug-in-units. The entire high speed central processor section of the FX-1 was built on 26 of these trays, 12 of which are identical. Figure 11 shows the two interconnection methods used on FX-1 trays. The first method uses 75-ohm Teflon-Insulated miniature coaxial cable, RG-187U. The second method uses a three-layer etched-wiring board with the center layer as a ground plane; the width of the etched lines on the faces, and the insulation thickness between them and the ground plane are controlled to produce 75-ohm strip transmission line. Connections to or through the ground plane are made with plated-thru-holes.

**Complete Machine**

Figure 12 shows a cross-section of the three-layer etched-wiring board. It is constructed by first etching two tray cards; one has the vertical wiring, the other has the horizontal wiring and the ground plane. Clearance apertures are etched in the ground plane where connections are not desired to the plated-thru-holes. The two cards plus two very thin cover layers are then laminated together and drilled. When the holes are drilled, the copper edges of the wiring lands and ground plane are exposed. Copper is then chemically deposited and followed by heavy electroplating. This copper on the two cover-layer faces is finally etched away leaving plated-thru-holes with small lands around them.

FX-1 was initially run using trays with coaxial-cable wiring. Eight of these have since been replaced by then etched-board equivalents with excellent results, and the remainder will be replaced in the near future.

**IV. Results & Conclusions**

The circuits described in this paper have been used to build a computer, the FX-1, which can perform instructions in less than one microsecond, and whose accumulator can add two 12-bit numbers in 160 nanoseconds. The 3500 transistor central processor has been in operation since July 1961. Debugging of the machine proceeded very rapidly. All signal waveforms were extremely clean and free from noise. Since initial debugging, the operation of the central processor has been reliable and entirely satisfactory.
Although the operating speeds were referred to as 50 megapulse per second; that is, 20 nanoseconds per register transfer, these speeds have not yet been obtained. At present, a 24-nanosecond register transfer rate is used because of the long gate-set up delay; however, modifications to the gate transistor circuit are now being studied which will allow operation at the stated speed.

The circuits and construction techniques employed are adequate for the construction of larger high-speed computers with improvement needed only in the flexibility of the level logic circuit and the component packing density.

V. Acknowledgement

The author wishes to thank Leopold Neumann and John Laynor who were deeply involved in the circuit design, Ellis Guditz who was largely responsible for the construction techniques employed, and to Dr. Donald Eckel whose group supported the transistor development contract.

VI. References


Table I

| Important Characteristics of L-5447 & T-2217 |

| Collector Voltage, $V_{CB}$ | -12 volts |
| Collector Voltage, $V_{CE}$ | -12 volts |
| Collector Voltage, $V_{CBO}$ | -7 volts |
| Emitter Voltage, $V_{BE}$ | -2 volts |
| Total Device Dissipation at 25°C | 35 mw |

Electrical Characteristics

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<td>v</td>
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<td>Base Input Voltage, $V_{BE}$</td>
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<td>430</td>
<td>mv</td>
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High Frequency Characteristics

| Output Capacity, $C_{o}$ | 1.5 | 3 | pf |
| Input Capacity, $C_{i}$ | 4.5 | 8 | pf |
| Gain Bandwidth, $f_{m}$ | 100 | 230 | mc |
| Gain Bandwidth, $f_{t}$ | 600 | 850 | mc |
| Hole Storage Factor, $K_s$ | 20 | 25 | nsec |

Table I

Fig. 1 Gain-Bandwidth vs Collector Current for the Philco L-5447 Transistor
Fig. 2 Basic Gated Pulse Amplifier
Fig. 3 Mixing Pulse Amplifier
Fig. 4 Input and Output of Mixing Pulse Amplifier

Fig. 5 50 Megapulse Flip-Flop

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Fig. 6 Input Pulse and Complementary Level Outputs of Flip-Flop

Fig. 7 Delay Line
Fig. 8 Variable Delay Unit

Fig. 9 Schmidt Trigger
Fig. 10 FX-1 Plug-In-Unit

Fig. 11 FX-1 Trays Showing Coaxial & Multilayer Etched Wiring
Fig. 12 Three Layer Etched-Wiring Cross-Section

Fig. 13 Overall View of the FX-1 Computer