TUNNEL DIODE STORAGE USING CURRENT SENSING

E. R. Beck, D. A. Savitt, and A. E. Whiteside
The Bendix Corporation
Research Laboratories Division
Southfield, Michigan

Summary

Tunnel diodes are attractive for use as the basic elements in high-speed random-access memories because of their fast switching speed and good environmental tolerance. A memory approach using tunnel diodes has been devised which is based upon destructive sensing of the operating current level in simple bistable elements. Each element consists of one tunnel diode and one resistor. This approach results in a near minimum of memory element complexity and of drive and bias power requirements. The immediate goal of the work reported is the development of a memory of somewhat over 1000 bits, able to operate from -55°C to +125°C at submicrosecond cycle times.

The feasibility of the overall memory concept, which is applicable to either bit or word organization, has been demonstrated by the operation of a test model. Test results indicate that a 200-ns cycle time is obtainable in a memory of 64 words of 24 bits each. Cycle time is roughly proportional to the square of the word capacity; correspondingly shorter cycle times can be obtained with memories of smaller capacity. With further circuit refinements it should be possible to operate a 64-word memory of this basic type at a cycle time of 100 ns or less over the temperature range of -55°C to +125°C.

Introduction

One of the most attractive immediate applications of tunnel diodes is in the construction of high-speed random-access memories. The tunnel diode offers the possibility of operating such memories over wide temperature ranges. This paper discusses a memory element that has been devised to make efficient use of the tunnel diode. Since this element provides no isolation between drive currents and sense output, the form of the matrix has been arranged to provide the required isolation. The matrix form is explained, and the techniques employed for driving and sensing with this form of matrix are discussed. The paper ends with some test results and conclusions.

Basic Design Choices

Basic Memory Element Component

The tunnel diode is attractive for use as a memory element because of its fast switching speed and good environmental tolerance. Potentially a low-cost device, the tunnel diode can be made with close initial tolerances on its parameters and on their variation with temperature. Tight packaging can also be used because of the tunnel diode's small size and low power consumption.

Semiconductor Types

With the exception of the tunnel diodes, only silicon semiconductor devices are employed in the circuitry. Either germanium or gallium arsenide tunnel diodes may be used in the basic memory elements; the switching speeds of the two types are comparable. Information received from manufacturers as well as tests of available units indicate that the necessary tolerances on parameters and their variation with temperature can be obtained. Gallium arsenide tunnel diodes are, however, capable of operation over a wider temperature range; roughly the same percentage of parameter variations occur from -55°C to +150°C as occur with germanium tunnel diodes from -55°C to +100°C. For this reason gallium arsenide units were adopted as soon as they became available. This choice must be qualified by the fact that the long-term stability of currently available gallium arsenide tunnel diodes is unsatisfactory. If this problem cannot be solved, germanium tunnel diodes must be used and the temperature range reduced.

System Organization

Word rather than bit organization was selected as being more suitable for the memory sizes of immediate concern and for the wide operating temperature range desired. It is possible to make a bit-organized memory using the concepts and circuits to be discussed, and in fact the feasibility of doing this was verified by...
the operation of a test model. However, no saving in selection and drive circuitry results from using bit rather than word organization in small memories, and the increased system tolerances afforded by the latter are clearly helpful in meeting the temperature requirements. Destructive readout was chosen because it was felt that the additional memory-element complexity required for a nondestructive readout capability was not justified by the somewhat higher speed obtainable.

The overall system organization used is the same as that of any word-organized memory with destructive readout. The system block diagram is shown in Figure 1 for reference purposes. It may be noted that for WRITE operations the sense outputs are brought directly to the bit-line drivers to avoid the propagation delay of the input-output register.

**Memory Element**

Destructive sensing of operating current level was chosen for the readout mechanism. This type of sensing allows the use of a bistable element with only two terminals and only two components, a tunnel diode and a resistor. Besides having the least number of components, this element allows the simplest matrix topology.

The form of the memory element is shown in Figure 2. The values of the bias voltage $V_{BB}$ and the resistor are chosen to make the circuit bistable. The state of the element is changed by increasing or decreasing, as appropriate, the voltage across the element to force operation to the desired stable state. The element voltage is changed by applying at points X and Y drive pulses of the type indicated.

With the diode polarity shown, a negative READ pulse applied at Y is used to switch the element to its high-current state, defined as the ZERO state. The increase in element current which occurs if a ONE is read is detected with the use of the transformer shown in Figure 2. A separate transformer is not required for each element. One transformer is actually shared by all the elements in a given bit position of all words.

Switching of the element to its low-current state for writing of a ONE is done on the coincidence of a positive pulse at Y and a negative pulse at X. To obtain larger tolerances with the WRITE operation the d-c bias is offset in the direction of the READ switching voltage. This bias offset also reduces the d-c power consumption, and permits the two opposite-polarity drive pulses at the Y terminal to be of nearly equal magnitude. The latter simplifies the generation of these drive pulses.

An inherent property of the element shown is the lack of drive-sense isolation. Currents produced by the drive pulses will produce noise signals in the secondary of the sense transformer which may be difficult to distinguish from the element output. Successful use of this type of element depends upon the cancellation of drive current obtained with the matrix configuration to be described below.

**Memory Matrix**

**Matrix Form**

The basic memory elements are connected in the matrix form shown in Figure 3 for word-organized selection of n words of k bits each. Each vertical matrix line is a word line and is connected to the Y terminals (see Figure 2) of all elements of a given word. Each horizontal matrix line is a bit line and is connected to the X terminals of all elements of a given bit position.

A single common sense transformer is shown in each bit line. The drive pulses of Figure 2 are supplied by the generators shown schematically in each line of the matrix. Only the generators in the selected lines are active, and the remainder may be considered to be shorted out.

**Memory Element Equivalent Circuit**

To understand how the driver currents are cancelled to obtain drive-sense isolation, it is helpful to consider an equivalent circuit for the memory element. Figure 4 shows that the memory element (a) may be represented by the equivalent circuit (b) consisting of a resistor $r$ in shunt with a current generator $I_s$. Resistor $r$ is the element incremental resistance, and $I_s$ is the difference in element current in the two stable states.

The justification for the equivalent circuit is illustrated by Figure 4(c). The memory element I-V characteristic is shown along with corresponding time plots of current and voltage waveforms. Assume that the element operating point is initially at point A. As the voltage across the element is increased from $V_{BB}$ to $V_H$, the
current through the element suddenly drops as switching from the high-current state to the low-current state occurs. This current change may be represented by the closing of the switch in series with the current generator in the equivalent circuit. The current generator provides a step of current which, if the element is allowed to remain in its new state, results in a change in the current drawn from the d-c bias supply. Similarly, an equivalent circuit for the element can be derived for the case where the initial operating point is at B and the voltage is reduced below $V_L$; this circuit differs from (b) only in the polarity of the generator $I_{g}$. If the voltage across the element is between $V_L$ and $V_H$ the element is simply represented by resistor $r$.

**Drive-Current Cancellation**

The drive-current cancellation can now be explained by referring back to the matrix of Figure 3. Current from the selected word-line driver is cancelled out of the sense transformers by simultaneous operation of the cancellation driver feeding the dummy "cancellation word" (resistors $r$) on the opposite side of the transformer primaries. Cancellation driver and word-line driver waveforms are identical. Selection of the proper cancellation word is made from the most significant bit of the address specified.

Current from the bit-line drivers is cancelled out of each sense transformer by applying this drive to the center tap of the primary winding. These transformers are placed in the center of the bit lines, with half of the word lines on each side of the transformer primaries. By replacing the elements with their equivalent circuits, it can be seen that the primaries are symmetrically loaded and the bit-line drivers produce no net current in the sense transformers.

**Matrix Equivalent Circuits**

For purposes of explaining the sense and driver requirements, the matrix may be replaced with the simple equivalent circuits shown in Figure 5. The matrix presents a load to the word-line and cancellation drivers equivalent to a resistor of value $r/k$ as shown in Figure 5(a). The matrix presents a load to the bit-line driver equivalent to a resistor of value $r/n$ as shown in Figure 5(b). Therefore the loading on the word-line driver is proportional to the number of bits per word, and the loading on the bit-line driver is proportional to the number of words.

The equivalent circuit of the matrix as a signal source for each sense circuit is shown in Figure 5(c). The current generator $I_g$ of the memory element being switched is shunted by the incremental resistance of all $n$ memory elements on the bit line. The equivalent sense transformer shown has a turns ratio of $1:2a$; the turns ratio of the center-tapped transformer actually used is $1:a$. The ratio $1:a$ is chosen for maximum transfer of power to the sense circuit. It can be seen that the matrix output power is inversely proportional to $n$, the number of words. Note also that the polarity of the $I_g$ generator will depend upon the location of the selected word; that is, to which end of the sense transformer primary the element is connected.

One of the main determinants of cycle time in a destructively-read memory is the delay in the rewrite loop. It can be derived from the matrix equivalent circuits, Figure 5(b) and (c), that the power gain required in the rewrite loop, and hence the rewrite loop delay, is proportional to $n^2$. The memory cycle time then varies roughly in proportion to the square of the memory word capacity.

**Drive Circuitry**

### Coupling to Matrix

The drive generators shown in the matrix of Figure 3 were indicated for ease of explanation. The drive voltages are actually introduced in series with the bias and memory elements by means of transformers as shown in Figure 6. The drive voltages required are low, on the order of 0.9 volt, and the required tolerances cannot be obtained directly with silicon transistor and diode logic circuitry at such levels. The drive transformers provide an efficient voltage step-down from convenient, easy-to-control logic signal levels to the matrix drive levels. Simultaneously, this approach provides the necessary low driver a-c output impedances.

### Drive Waveforms

Two cycles of the required drive-pulse waveforms are shown in Figure 7. These essentially repeat the waveforms shown in Figure 2 except that an additional bit-line drive pulse is indicated with dotted lines. Since word-organization is being employed, reading is accomplished by the negative word-line pulse alone. Writing a ONE, however, requires the coincidence of the word-line and bit-line pulses. Writing a ZERO is accomplished by delaying the
A delayed bit-line pulse must be used when a ZERO is being written because the drive voltages are a-c coupled to the matrix lines. If a pulse were not applied on the bit line every cycle time, whether a ZERO or a ONE was being written, the pulse duty cycle would be variable and dependent upon the sequence of memory operations. Such a variable duty cycle would make the effective matrix bias voltage variable, reducing the bias-supply tolerances. Note that by employing equal-area read and write pulses on the word line the average value of this waveform can be made equal to zero for each cycle; therefore there is no duty cycle problem on this line.

Drive Circuits

The pairs of alternate-polarity drive pulses required for the word lines are obtained by differentiating a rectangular OPERATE pulse provided by the word-line pulse generator. (See Figure 1). Only unipolar pulses need then be handled by the word-selection circuitry. Each word-line driver consists of a tuned transformer driven by a diode AND gate as shown in Figure 8. The transformer is critically damped and the write pulse amplitude is clamped. The last level of address decoding is also done in this circuit.

The bit-line driver is shown in Figure 9. Transistor Q1 is a pulse amplifier and transistor Q2 provides low-frequency feedback for control of the pulse area. A clamp voltage is used to control the pulse amplitude, and resistor RT provides temperature compensation. The input to this circuit is supplied from a three-input OR gate which in turn is fed from three AND gates. The AND gates are controlled by the sense circuit outputs, the input-output register and the OPERATE READ command. (See Figure 1).

Level Restoration

The sense circuit must detect the presence of and amplify the current step Isg (of the matrix equivalent circuit) produced by a switching memory element. Each time another element switches, another current generator can be considered to be added in shunt with the one shown in the equivalent circuit of Figure 5(c). The level of the matrix output at any time then will vary, depending upon the polarity and spacing of the previous output step waveforms. It is therefore necessary to restore the matrix output level to zero after each new step of current occurs.

Level restoration is achieved in a manner similar to differentiation by the use of a short-circuited delay line connected across the sense transformer secondary. The manner in which level restoration is accomplished with a short-circuited delay line is illustrated in Figure 10. In this figure, eg and Rg represent the equivalent circuit of the matrix as seen from the sense transformer secondary, and Rl represents the input impedance of the sense circuitry. The value of the parallel combination of Rg and Rl is made equal to the delay-line characteristic impedance R0. Step waveforms from the matrix are then converted to rectangular pulses as shown. The pulse width is equal to twice the delay time Td of the line. In general, a rectangular pulse is generated for each step of matrix output, and the pulse polarity is the same as the step polarity. The effect of the circuit, then, is to restore the matrix output level to zero before the next signal arrives. This permits an amplitude level discriminator to determine if a signal is present.

Level Discrimination

In addition to the step current waveforms resulting from the switching of memory elements, the matrix also produces some noise. Noise results from the imperfect cancellation of the drive currents in the matrix. The noise resulting from the word-line driver is relatively low compared to the matrix output signal level, because the cancellation element and driver can be matched closely to the active words and drivers.

The noise produced by the bit-line drivers, however, depends upon the match between the incremental resistances of all elements on one side of the sense transformer primary and the resistances of all elements on the other side. The noise level then is proportional to the matrix size in words and can be significant compared to the matrix signal for memory sizes of interest. However, this noise is produced only during the WRITE operation, when sensing of the matrix output is not performed.

Because of the presence of noise in the matrix output, it is desirable to use a level discriminator in the sense circuits. Since it is
undesirable that a response be generated during the WRITE operation (because this could result in a recovery time problem at short cycle times), the discriminator is strobed during the READ operation. Since the pulses produced by the level restorer may be of either polarity, a bipolar level discriminator is required. The circuit employed to meet these requirements is shown in Figure 11(a).

The bipolar discriminator circuit is essentially two tunnel diodes in parallel, biased by a current source \( I_B \) to a point just below their peak currents. The output voltage is initially low. An input pulse is fed to the diodes through the center-tapped transformer. As a result a positive pulse appears in series with one tunnel diode and a negative pulse is in series with the other. If the input pulse exceeds the discrimination level, both diodes switch to their high-voltage state, and the output voltage goes high. Strobing is accomplished by using a pulse bias which is turned on only during the read operation.

The circuit operation is explained by Figure 11(b) and (c). Figure 11(b) shows the situation when the input voltage \( e_p \) is zero. The solid curve is the I-V characteristic of one diode, and the dotted curve is the characteristic of the two diodes in parallel. With the bias \( I_B \) shown, the initial operating point is A. Figure 11(c) illustrates the effect of \( e_p' \). The characteristic of one diode is shifted to the left and the other one to the right. The characteristic of the two in parallel, shown by the dotted line, then has a lower peak current than when \( e_p \) is zero. If \( e_p \) is large enough, the equivalent peak current is reduced below \( I_B \) and the operating point switches to B, producing an output signal.

Amplification

In addition to the functions of level restoration and discrimination, the sense circuits must provide amplification. Because of the shunting effect of all the other memory elements of a bit line on the output of the one memory element that switches, the amount of gain necessary to allow the sense output to operate the input-output register increases with the memory size.

To sense the low-power matrix output, a sensitive discriminator is required. Discriminator sensitivity is inversely proportional to the peak current of the discriminator diodes. Accordingly, low-peak-current units are employed. The discriminator is followed by two stages of tunnel-diode amplifiers of the analog threshold OR-gate type; successive stages use diodes having higher peak currents. All stages are biased by the same pulse supply, and inter-stage coupling is accomplished with high-speed diodes.

The switching time of a tunnel diode is approximately inversely proportional to the diode peak current. As a result, the sense delay contributed by the discriminator is proportional to the sensitivity. It was found for the 64-word memory that the delay with a single-stage video transistor pre-amplifier before the discriminator was less than that with a discriminator sensitive enough to operate directly on the matrix output. The discriminator employs two 0.5-ma tunnel diodes, the succeeding stage uses a 4.7-ma diode, and the output state employs a 22-ma diode.

Experimental Results

The feasibility of the concepts and circuitry described has been proved with a trial system which simulated a memory of 64 words of 24 bits each. Two words of active memory elements were used, and the remainder were simulated by resistors. The first tests were made with two active word-line drivers and one complete rewrite loop consisting of a bit-line driver and sense circuit. The loading and source-impedance effects of the remainder of the drivers were simulated.

The memory was operated in a repetitive READ-ONE, WRITE-ONE sequence at a cycle time of 280 ns. The rewrite loop was closed and a bit was circulated in a READ-ONE, REWRITE-ONE sequence at the same speed. Based upon the measured delays in the rewrite loop, it is estimated that the present circuitry is capable of running at a 200-ns cycle time. The additional delay in the 280-ns cycle was due to limitations in the word-line pulse generator.

Figure 12 shows driver and sense-output waveforms for a READ-ONE, REWRITE-ONE sequence; the waveforms are identical for a READ-ONE, WRITE-ONE sequence. (The presence of a sense output pulse indicates that a ONE has been read during this cycle by the word-line READ (negative) pulse. Since the bit-line driver pulse is in coincidence with the word-line WRITE (positive) pulse, a ONE is being written at this time.) The waveforms show a 60-ns delay in the sense circuits and a 40-ns delay in the rewrite logic.
Figure 13 shows the matrix and sense circuit outputs for both READ-ONE, WRITE-ONE (a) and READ-ZERO, WRITE-ZERO (b) repetitive memory operations. Two memory cycles are shown and the word-line driver waveform is included for a time reference. The matrix-output waveform includes the effect of the sense-circuit level restorer. A comparison of the matrix output waveforms of (a) and (b) shows the excellent ONE-to-ZERO ratio achieved. As stated before, the output level is inversely proportional to the number of words in the matrix. For the 64-word memory being operated here, a ONE produces a 20-mv pulse across the 250-ohm sense-circuit input impedance.

Limited temperature tests have been performed on the driver circuitry, and the results indicated that the tolerances required on the drive pulses can be met over the temperature range -55°C to +125°C. Figure 14 is a photograph of the test system chassis which consists of a base ground plane into which circuit cards are plugged. Two cards are shown in place, one of which is a digit plane card. A partially assembled digit plane is shown in the foreground.

Conclusions

The overall memory concept used, which is based on current sensing, appears to be one feasible approach to construction of a high-speed random-access memory. The approach results in low drive and bias power requirements. In the model discussed, the maximum d-c power consumption per bit is 1 mw; the maximum peak drive power per bit (for writing a ONE) is 1.6 mw. A cycle time of 200 ns is obtainable for a memory of 64 words of 24 bits each with present transistor driver circuitry. The cycle time varies roughly with the square of the number of words; correspondingly shorter cycle times can be obtained with smaller memories. The circuitry has been designed to operate from -55°C to +125°C, and uses only silicon diodes and transistors and gallium arsenide tunnel diodes.

The simple form of the memory element allows a high degree of matrix miniaturization. To show what can be done, the 16 by 16 array shown in Figure 15 was constructed, using tunnel diode packages expected to be available and small metal-film resistors.

Replacement of transistor drivers with tunnel-diode circuits is an attractive possibility. Drive pulses of the required amplitude can be obtained with a single tunnel diode switching between its low- and high-voltage states. Tunnel diode driver circuitry is simpler and more compact than the transistor-diode circuitry currently used. It should also be faster and, in particular, should greatly decrease the delay in the rewrite loop. It is believed that a 64-word memory will then be capable of cycle times of 100 ns or less from -55°C to +125°C.

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References

Figure 1. MEMORY SYSTEM BLOCK DIAGRAM
Figure 2. BASIC MEMORY ELEMENT
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Figure 4. MEMORY ELEMENT EQUIVALENT CIRCUIT

Figure 5. MATRIX EQUIVALENT CIRCUITS
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Figure 7. IDEALIZED DRIVE WAVEFORMS
Figure 8. WORD-LINE DRIVER
Figure 9. BIT-LINE DRIVER

Figure 10. DELAY-LINE LEVEL RESTORER AND WAVEFORMS
Figure 11. BIPOLAR DISCRIMINATOR
Figure 12. DRIVE AND SENSE-OUTPUT WAVEFORMS

(a) READ-ONE, WRITE-ONE OPERATION
MATRIX OUTPUT (50 MV/CM)
WORD-LINE DRIVER (1 V/CM)
SENSE OUTPUT (0.5 V/CM)

(b) READ-ZERO, WRITE-ZERO OPERATION
MATRIX OUTPUT (50 MV/CM)
WORD-LINE DRIVER (1 V/CM)
SENSE OUTPUT (0.5 V/CM)

TIME SCALE - 40 NS/CM

Figure 13. MATRIX AND SENSE CIRCUIT OUTPUT WAVEFORMS
Figure 14. MEMORY TEST MODEL

Figure 15. POSSIBLE MEMORY MATRIX CONFIGURATION