DESIGN AND DEVELOPMENT OF A SAMPLED-DATA SIMULATOR
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Introduction
This paper describes the design and development of a sampled-data simulator (a special purpose analog computer) constructed recently at Space Technology Laboratories, Inc. (STL). The device was developed to simulate missile and spacecraft control system problems containing both continuous and sampled information. The machine has increased the speed of simulation, and decreased costs of operation.

Recent developments in space technology requirements, particularly of systems containing sampled or discrete data, present a class of problems requiring simulation of both sampled and continuous information containing both high and low frequencies. To accomplish this type of simulation on an analog computer, the sampled-data circuits which are described here were devised. The sampled-data channel consists of two zero-hold circuits in cascade, the first amplifier sampling the continuous input signal and the second amplifier presenting the stored information. Performance accuracy, which is within 0.01 percent of the desired value, was achieved by employing the special design and packaging techniques described.

Background
Sample-and-hold techniques have been in use on analog computers for a number of years. Several papers report on the use of operational amplifiers and relays for the simulation of sampled-data systems. The same method has been used for sample-and-hold operation in specialized analog integration.

Of the various methods used to simulate the sampled-data system with analog equipment, three had previously been exploited at STL, all with significant drawbacks.

The first method used a digital computer for the sample-and-hold operation and the solution of difference equations. It employed a combined simulation system comprised of an analog computer, the Univac 1103A digital computer, and the Addaverter analog-to-digital and digital-to-analog converter. This method was costly for problems requiring only a small amount of digital computation.

In a second method, the Addaverter was used by itself as a sample-and-hold simulator, with A-D and D-A channels connected in series to obtain and store the present and past values of a periodically sampled variable from the analog computer. This method was time-consuming and employed an excessively complex device for relatively simple operations.

A third method used analog computer amplifiers and relays wired on a standard patchboard as sample-hold circuits. Although the method was inexpensive, the amplifiers and sampling relays did not have performance characteristics that made high-speed sampling possible and the number of components needed for such circuits was excessive.

Accordingly, investigations were made of methods to overcome the disadvantages of using analog computer components for sample-hold circuits. It was determined that by limiting the maximum sampling frequency to 100 cps, a high-speed relay could yield the desired performance. An investigation of the rise time and drift characteristics of currently available amplifiers showed that components were available with adequate specifications for a sample-and-hold circuit operating in the calculated frequency range of 0.05 to 100 cps.

On the basis of these studies, a prototype unit was fabricated and proved sufficiently successful in actual problem solution to justify the construction of the full-scale simulator.

Description of Basic System

Sampled-Data Channel
The principal requirement for a sampled-data channel with zero-order hold is to sample a continuous input signal periodically so that its output signal changes magnitude in a stair-step manner. The approach taken to satisfy this requirement was to use an analog computer operational amplifier, passive elements, and a high-speed relay connected as the sample-hold circuit. (Figure 2)

The circuit becomes a first order lag when the relay contacts are closed and the output charges to the amplitude of the input in an exponential manner. The lag time constant is equal to the value of RC. With the relay contacts open the amplifier is an integrator with no input E(t), and the output E(t) is equal to the charge on the capacitor C. The circuit will hold the charge until the relay is again operated and the capacitor is charged to a new voltage level. The RC value can be minimized until equal to the amplifier rise
time, which was chosen to be a factor of 10 smaller than the time the relay contacts are held closed.

It was necessary to have a means whereby the basic channel could be connected to other channels and the signal delayed up to six sampling periods. Rather than using cams and switches to sequentially drive the sample relays, two sample-hold circuits of Figure 2 were cascaded to give the sample-and-hold or sampled-data channel shown in Figure 3.

In the sample-data channel, the Sample Amplifier output is stored in the Present Amplifier circuit to prevent loss of the information when the next Sample pulse operates the Sample Relay. Transfer of the signal is accomplished by delaying the Sample pulse to the Present relay by a period having a range from the minimum time the relay is closed (a factor of 10 greater than the RC value) to the maximum of one second, the maximum time being determined by the delay-flop (monostable multivibrator) design. This method permits cascading of channels to obtain a Sample period delay per channel plus a small Present delay. Noticeable effects do not occur in most problem simulations when the delay is set at its minimum value.

System Controls

To operate two groups of channels at different related frequencies, the groups running at the higher frequency are operated as described, but the input for the lower frequency must be obtained by dividing the higher frequency \( f_0 \) by some integral number.

To instrument difference equations directly at a patchboard, summing amplifiers and coefficient potentiometers are required. Mode controls for the summing amplifier relays and the sample-and-hold relays include potentiometer setting (Pot Set), initial conditions (IC) on Present amplifiers, sample-hold amplifier integrator hold (Hold), and the start of computer operation in synchronism with the first clock pulse (Compute). Such controls, with the digital logic required for pulsing the sampling relays, determined the basic system indicated in Figure 4.

In Figure 4, note that the remote analog computer can control or be controlled by the simulator as required. However, the simulator can be operated independently from its own control panel. The purpose of the Hold Synchronizer (start control) is to start the simulator in the Compute mode coincident with the first sample pulse after the operator has changed the mode switch to Compute. This prevents the occurrence of a fractional interval during the first sample period. All sample and present relays are energized to clear an initial input voltage just before the simulator is in the Compute mode by the automatic clear circuitry or they can be energized at any time by depressing the master clear switch. The frequency divider (counter) reduces the frequency for the low frequency group pulse formers if so desired. The Clock is a low frequency square wave generator that is connected to the Hold Synchronizer. The output pulse width of the Hold Synchronizer is reshaped in the pulse unit before the relay driver and closes the sampling relay contacts for a period (10 RC time constants) that will insure the desired accuracy of the sampled signal.

Design Considerations

The major problems encountered in the design tasks were direct consequences of using both analog and digital components in the same system. Previous experiments with diode gating circuits as sampling devices in sample-hold circuits had proved that these diode gate circuits introduce excessive noise into the amplifiers, that "open" impedance is too low, and that a well-regulated power supply is required for biasing the diode gates.

Therefore, objectives of sampling relay circuit design were to select a high-speed relay, and to design (a) a compatible relay driver circuit, (b) a pulse-former circuit to shape the width of the sampling pulse, (c) a present delay circuit to operate the present relay after the sample relay is actuated, and (d) pulse control circuits to start the operation of sampling relays with the analog computer control mode relays.

Sampling Relay Circuitry

Tests of a chopper as a sampling relay in a sample-hold circuit showed that the relay operated up to 1200 cps without any noticeable effects in the dwell time or phase-lag. The relay is a polarized single-pole, double-throw, non-resonant switch that provides break-before-make action in synchronism with the current-wave of the driving source. The mechanism is housed in a metal case having a plug-in header and captive, locking external shield. The unit fits a standard skirted 7-pin socket.

Electrical performance and life of contacts are closely related to the characteristics of the circuit into which the relay is used. Standard contact-rating is 3 volts, 2 milliamperes, resistive load. Contact voltage could be restricted by using a diode limit circuit on the amplifier grid.

To drive the relay at the sampling frequency of the clock source, a driver circuit (Figure 5) was designed. The circuit is basically transistorized switches that operate from the output of a pulse-former. A negative pulse causes \( Q_1 \) to conduct, the current is forced from ground up through the coil, and the contacts (6 and 7) are closed for the duration of the sampling pulse. A positive pulse forces current in the opposite direction, closing contacts 1 and 7.

In order to provide sufficient time for the capacitor in the RC network to charge to within 0.01 percent of the sampled input level, the relay contacts must be closed for a duration of time greater than the RC value. The pulse-former
A frequency divider is used to divide the pulse frequency from the Hold Synchronizer to the pulse-formers for the sample and present relays. Each of the two ten-point decade counting units has a selector knob allowing the set-in of any desired value from 0 to 9, the actual number chosen being indicated by the selector knob dial. After presetting, the coincidence output signal is generated whenever the input signal count agrees exactly with the chosen preset number. The two units permit a total count and preset number range from 0 to 99.

A clearing circuit consists essentially of a control relay whose contacts apply voltage to the relay driver units. The unit contained sampling relays, passive networks, control relays (Pot Set, IC), Hold Synchronizer, frequency divider (counter), and digital logic. Four amplifiers were cabled from the analog computer to the unit for the two sampled-data channels. The prototype unit was used successfully in many problem simulation studies.

Amplifier Selection

The prototype unit sampling frequency was limited by the amplifier performance characteristics. Amplifiers made by various analog computer manufacturers were tested, and an operational amplifier eventually was selected for sample-hold applications. In addition to the general requirements of output current, gain, frequency response, and phase shift, it was found that the amplifier integrator drift during a hold time of 4 seconds and with a 0.001 microfarad feedback capacitor is 2 millivolts, that its noise is 5 to 10 millivolts, and that amplifier rise time is 40 microseconds.

Simulator Specifications

At this point simulator specifications were formulated upon performance of the previously designed circuits, high-speed relays, and the selected amplifier, after which development was initiated.

The simulator has 12 sampled-data channels, each consisting of two amplifiers in cascade. The first amplifier samples on command of a Sample pulse. The second amplifier will sample on command of a Present pulse. In addition to the sampled-data channels, 12 summing amplifiers and 20 coefficient potentiometers are available to make possible the instrumentation of difference equations directly on the simulator patchboard.
The simulator is a self-contained unit with its own power and relay supplies, controls, and patchboard. An insulated patchboard was used for inputs and outputs of system components.

A 0.001 microfarad capacitor is employed in the sample and present amplifier feedback. The maximum allowable drift specified was 2 millivolts in 4 seconds, or a rate of 0.5 millivolt/second. The noise level measured at the patchboard is less than 10 millivolts, a good value since the patchboard is not shielded.

Logic elements are transistor type with inputs and outputs brought out to the patchboard. These elements, with logic levels of -3 and -11 volts, include flip-flops, delay-flops, "and" gates, "or" gates, emitter followers, blocking oscillators, Schmidt triggers, and level triggers. The flip-flops, delay-flops, and blocking oscillators trigger on 5.5 volts in at least one microsecond. A falling waveform will not trigger any of these circuits, regardless of voltage or slope of signal.

The maximum and minimum delay of the present pulse are one second, and 500 microseconds respectively; a delay-flop is employed. Adjustments for varying the delay time are placed on the left side of the patchboard panel, one for each of the four present pulse former units. External capacitors may be added by means of banana jackets located on the chassis housing the pulse former units, accessible from the rear of the control cabinet.

Amplifier Circuit

Each amplifier grid, output, and overload wire is cabled to the control cabinet for connection with passive networks, operational and sampling relays, and to indicate an overloaded amplifier at the central overload indicator on the control panel. The plate and filament voltages are cabled to the amplifier chassis within the amplifier cabinet. The summing amplifier networks have four 50K ohm input resistors and the present amplifier has one 50K ohm input resistor.

To indicate that an amplifier is in an overload condition, a light on the control panel is turned on and an audio alarm is actuated. The alarm has both tone (frequency) and volume adjustments.

Simulator Control Circuits

Control panel switches operate relays that turn on or off the filament, plate, and reference voltages for the simulators. As the switch is pressed a light indicates the "on" condition.

In order to read out the voltage of power supplies, trunk lines, potentiometer arms, and the sample, present, and summing amplifier outputs, a pushbutton selector system was designed. A selector switch of 100 points and a relay of 50 points connected in series form a 150 point system. Points 1-99 are selected by the switch and points 100-150 are selected by the addition of the relay.

The mode controls are relays operated by control panel switches. The operating mode is indicated by a light on the surface of each switch.

Simulator Development

Patchboard Layout

The patchboard is an insulated, 816-hole board. Colors were applied to the board by an inexpensive photo-emulsion process rather than by the standard but expensive silk-screening method. Colors denote inputs, outputs, ground, etc. All inputs, outputs, trunk lines, and multiple points are numbered for clear identification (Figure 8).

Amplifier Installation

All amplifier chassis are mounted in the amplifier cabinet (number 23 shown on the right side of Figure 9).

Amplifiers are packaged in groups of four (or quad) and three groups are mounted in one amplifier chassis. Figure 9 shows the following system components in the amplifier cabinet (from top down): 12 Sample amplifiers, 12 Present amplifiers, digital voltmeter, clock, filament transformers (behind shelf), 12 Summing amplifiers, and plate supply unit.

Oven Fabrication

It was necessary to locate the oven as near as possible to the patchboard (as shown in the control cabinet in Figure 9) to minimize noise pickup. An oven thermostat, having a set point of 100°F, controls the temperature environment for the passive networks. Heat is generated by power resistors and the air is circulated by a small blower mounted on the back of the oven. Capacitors are adjustable through access holes in the front of the oven. The connections for the plug-in networks are also mounted on the front of the oven to facilitate wiring.

Potentiometer Panel

Twenty coefficient, hand-set potentiometers with input switches and arm fuses were assembled on a panel and mounted directly above the patchboard panel. Pots are ten-turn Helipots, with 30K ohm resistance and 0.1 percent linearity.

Control Panel

Figure 10 shows the control and patchboard panel. On each side of the patchboard are dials and switches for selecting the capacitor value for the present pulse unit delay (left side) and spare...
delay-flops (right side). The following controls are shown on the control panel: power-controls, flip-flop clear lights, divider (counter) clear light with frequency indicator lights and selector knobs, function switches, amplifier overload lights, readout (address) selector pushbuttons, Level Trigger polarity selection knobs, overload test switch, master clear switch, switch for connecting digital voltmeter to address selector or patchboard terminal, and control mode switches for Slave, Pot Set, IC, Hold, and Operate.

Wiring

The most time-consuming phase of the development program was the wiring of the simulator. Extreme care was taken to shield wires carrying d-c voltages from those carrying pulses and a-c power. A carefully designed ground system was used to prevent the introduction of a-c noise signals to the input of the high gain operational amplifiers in the simulator.

Signal Ground. The amplifier grid wire is shielded to prevent electrostatic induction of noise. The shield is used as the ground for only those wires it shields, and is tied to another shield only at one point where both are grounded. A copper bus bar is located behind the patchbay for connecting all types of grounds, except the a-c neutral. This bar is then connected to the facility earth ground by three No. 8 size wires to cause the bar to act as the earth ground of the simulator. In addition, the cathode input stage of the amplifier stabilizer has the cathode ground brought directly to the system earth ground to minimize interaction by amplifier channels.

Power Ground. All power currents return only through power ground leads. At no place is the power ground connected to the signal or chassis ground on the amplifiers. However, the power ground is connected to these grounds on the earth ground bus mentioned above.

Chassis Ground. The chassis of all units are grounded through the slides which hold them in the cabinet, and the panel screws. The cabinets are in turn grounded to the earth ground bus in the control cabinet. Each unit as well as the whole system is then in effect enclosed in a Faraday shield.

a-c (Neutral) Ground. The a-c ground, sometimes called an industrial ground or the a-c neutral, is the fourth wire of the three-phase power brought to the computers in the facility. To prevent a-c noise pickup in the equipment, this ground is not connected to any of the above grounds but serves only for the return of a-c current.

System Performance Data

Typical new system testing was performed before the simulator was put into operational use. However, some impossible-to-anticipate difficulties were not encountered until the machine was actually used for several different problem simulations. The data given in this section prove the degree of accuracy with which the system met specifications.

Test Problems

The most essential requirement of the sampled-data channel is that each channel cascaded to the first channel give a sample period delay. This was investigated by imposing a sinusoidal or triangular waveform at 0.01 cps on the input and a sample period of 5 seconds to the first channel, and recording the input and outputs of the three channels cascaded (Figure 11). Although the amplitude of the sampled signal appeared identical as it passed through each cascaded channel, a special circuit was mechanized to detect the amplitude error in the output of each channel when six channels are cascaded. Each sampled-data output was compared to the input, with the error signal recorded. The input signal was 12 volts d-c. In Figure 12, the maximum error recorded is 20 millivolts in the output of the sixth channel, which indicates some of the error is accumulated.

Again, the output signal variation, with the input signal varied in frequency and the sampling frequency held constant, was investigated. A triangular and then a sinusoidal input signal of 100 volt amplitude was varied in frequency from 0.05 to 50 cps in increments of 10 cps. The sampling frequency was constant at 100 cps. As viewed on an oscilloscope, no apparent change in the output waveform was noted.

Integrator Drift. The integrator drift rate is of prime importance during the lowest sampling frequency selected. To maintain the accuracy given in the specifications required the drift rate to be 0.5 millivolt/sec during a sampling period of 4 seconds. In addition, the specifications required the maximum drift to be within 20 millivolts during the maximum sampling period, or 0.01 percent of 200 volts full scale.

Integrator drift is due mainly to two factors: (a) the capacitor leakage in the circuit while holding or storing the sampled signal, and (b) the amplifier offset voltage caused by input-tube grid current. Precautions were taken in wiring the simulator to minimize possible capacitor leakages in the system.

The measured drift rate of the system met the required specification only after careful adjustment. However, a drift rate of 3 millivolts/second, which could be obtained with relative ease, was used to determine the lowest sampling rate.

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Noise Level. The output noise level has a high frequency content well within 10 millivolts peak-to-peak, while the low frequency is within 5 millivolts peak-to-peak. In initial bench tests of the circuit, the total noise level was within 4 millivolts.

Transient Response. It was desirable that the amplifier transient response have a rise time of 50 microseconds. The rise time, measured from 10 to 90 percent of the final value, was found to be 50 microseconds. This satisfies the specification that the amplifier rise time be equal or less than the RC network time constant.

Crosstalk and Random Triggering

The crosstalk measured at the patchboard is only 20 millivolts when the output of one amplifier is $100 \sin \omega t$ and the input of the measured amplifier is open.

Occasionally, while checking the performance of the simulator, fractional sampling would occur. An investigation revealed that this occurred whenever test equipment on the simulator a-c line was turned on or off. The source of the trouble was traced to the delay-flop. It was found that noise or transients would change the output state of these units, which are used throughout the system wherever a delay is desired. Since the Hold Synchronizer has a delay-flop the problem may be started prematurely, resulting in fractional interval of the first sample period. Functional sampling may also occur at any time during the problem as a result of a false or undesired pulse triggering the delay-flop in the pulse former units. In order to eliminate this problem, a redesign of the delay-flop is under consideration at present.

Conclusions

The results of performance evaluation tests indicate the lowest sampling frequency (within 0.01 percent accuracy) to be 0.125 cps when critical adjustments are not made. This is considerably higher than the calculated frequency of 0.05 cps. One method to lower the limit to 0.05 cps would be to lower the maximum sampling frequency. This would allow an increase in the value of the feedback capacitors, thus reducing the amplifier drift. The sampling pulse width would, of course, be correspondingly increased. Amplifier rise time could then exceed its previous maximum limit of 50 microseconds, since no advantage accrues from restricting it below the RC time constant of the network.

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References


Figure 1.

Sampled-Data Input-Output Signal with Sampling Pulses.
Figure 3. Sampled-Data Channel.

Figure 2. Sample-Hold Circuit.

Figure 4. Basic Sampled-Data Control System.
Figure 5. Relay Driver Circuit.

Figure 6. Pulse Former Circuit.

Figure 7. Block Diagram of Hold Synchronizer.
Figure 8. Patchboard.

Figure 9. Simulator Control and Amplifier Cabinets.
Figure 10. Control and Patchboard Panels.
Figure 11. Input and Outputs of Three Cascaded Channels.

Figure 12. Comparison of Input and Outputs for Six Cascaded Channels.