MICRO-SYSTEM COMPUTER TECHNIQUES
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ABSTRACT

This paper briefly describes some of the problems encountered in building very high-speed (nanosecond) computer systems. A number of the techniques developed for a tunnel diode computer are described in detail, although it is emphasized that the difficulties are due to the operating frequency, rather than to any characteristic of the switching device.

Among the items discussed are ceramic circuit wafers with fired-on metallized circuitry and ground plane; vacuum deposited rod resistors developed for this program; a grooved channel wiring assembly which holds the wafers; a new approach to a flexible transmission line; and a tunnel diode memory plane.

INTRODUCTION

As computers are made faster, the electrical requirements of the packaging system become more severe. Development of the Project LIGHTNING, 1000-megacycle, tunnel-diode computer has shown three main problem areas:

1. Wiring delays become significant.
2. Signal waveform distortion is greatly increased.
3. Signal crosstalk is greatly increased.

From the manufacturing point of view, the packaging scheme must be practical, which means relative ease of fabrication or, in other words, high yield. The wiring should also be flexible, so that leads may be opened, gates tied up, and signals simulated during the debugging phase.

High manufacturing yield and electrical flexibility indicate that the basic circuit unit should be small, since both yield and flexibility decrease rapidly if the basic unit consists of a large number of components. This is especially true if tight component tolerances must be maintained.

The geometrical shape of the basic circuit unit is primarily dictated by its electrical requirements. These must include not only the placement and interconnection of circuit components, but must allow a measure of freedom and ease in interconnecting a multitude of these basic circuit units. High component densities of a circuit unit cannot be utilized if its construction fails to provide electrical and mechanical interconnection flexibility to other units, a consideration which some miniaturization schemes lack, and which cannot be sufficiently emphasized.

LOGIC CIRCUITS

Our present logic unit consists of a wafer with the tentative dimensions of 0.775 inch by 0.400 inch, as shown in Fig. 1. The material of the wafer is alumina, with a thickness of 0.020 inch. Terminal pads provided on three sides are used to connect the wafer circuitry with other similar units.

Utilizing three sides and a relatively high number of pads facilitates the layout of the circuitry on the wafer, since crossover of lines must be avoided. The back of each wafer is copper plated and is grounded. Metallized lines on the wafer are 0.025 inch wide and, with the dielectric of the wafer and its copper-plated and grounded back, form a transmission line (strip transmission line). Vacuum deposition of resistors directly on the wafer could be done since these techniques are well known. However, our circuitry requires one percent tolerances and this coupled with the fact that we may need six to nine resistors of three or four different values on a single wafer, places an unnecessary strain on experimental circuitry. Therefore, a ceramic rod resistor, 0.020 inch diameter by .100 inch long, was developed for the program. Each end of the resistor is metallized so that it can be soldered to the circuit pad; the resistive material is vacuum deposited on 0.060 inch of the body and covered with a deposited inorganic film and a silicone resin to avoid damage during handling and soldering.

An example of an actual experimental circuit is shown in Fig. 2. It is a dual-locked-pair circuit and consists of four tunnel diodes and eleven resistors. Reactive components are not required in this circuit. However, small inductances can be formed by loops. For inductance values which cannot be achieved by loops, air coils could be used, but their utilization in high-speed circuitry is not extensive. Capacitors are soldered...
2.4 to the circuitry in the form of small ceramic pieces which have a high dielectric constant and are metallized on both sides. Since all components can be tested prior to assembly, the yield is high.

Consideration must be given to testing the assembled wafers at full operating speed. The test jig must provide electrically smooth connections between the test equipment and the terminal pads of the wafer. Fig. 3 shows such a jig. The wafer is placed in the opening near the top surface of the jig where spring contacts ground the copper-plated back of the wafer; the connecting wires are soldered to the terminal pads of the wafer and then guided in channels to coaxial connectors mounted at the rim of the jig. The test equipment is connected here using conventional coaxial cables. The wires in the channels and the channels themselves are designed to maintain a uniform impedance level and freedom from crosstalk.

To form an assembly with a multitude of wafers, provisions must be made to hold the wafer in place and provide the numerous interconnections. At high switching speeds, the requirement of suitable electrical interconnections between the wafers overrides all other considerations. These interconnections are no longer short in comparison to the wave length of the frequencies which they carry and, therefore have to be treated as a communication network; wiring delays, signal waveform distortions and crosstalk become significant design considerations. The final speed of the computer will be influenced by the speed with which this "communication network" can distribute the internal signals at the right time without major distortion and crosstalk to the individual circuits.

Printed circuit techniques have various electrical disadvantages which can usually be overcome in medium-speed computers but which cannot be tolerated in a high-speed (nanosecond) machine. On printed transmission lines, there is appreciable crosstalk between closely spaced parallel wires since the ground plane structure which is needed to electrically separate such circuits is prevented from doing so by the dielectric sheet. Crossovers of printed circuit lines are complicated and introduce electrical discontinuities and additional crosstalk. Non-uniformities in the wiring or associated fittings may cause spurious resonant modes in the relatively large dielectric sheet.

A shielded coaxial transmission line has none of these disadvantages; it provides a physical path with uniform inductance and capacity per unit length and has minimum crosstalk.

This transmission line concept is used in the channel wiring assembly. The basic idea is to place an insulated wire in a metal channel of a slab-like structure having two or more channel patterns. The same channels also are used to hold the wafer in place. The terminal pads of the wafer line-up with these channels, so that each wire remains in its channel until it reaches the proper wafer pad. The electrical connection of the wire to the wafer is done by stripping the wire insulation and soldering the wire to the terminal pad on the wafer.

The diameter of the conductor, dielectric constant and diameter of the insulation contribute to the characteristic impedance of the line. With each wire in its own channel, crosstalk is minimized. Further shielding can, however, be achieved by painting the top of the channel with conductive epoxy. Where the same pulse arrives at separate circuits at different times because of propagation delay, both wires can be pre-cut to the longest length and the slack to the closest circuit taken up by running it back and forth in channels.

The channels are arranged in a 0.050-inch pattern which permits flexible wiring and still maintains transmission line characteristics. Where wires must cross each other, a hole is drilled in the channel and one of the wires goes through this hole into a channel on the reverse side and returns at a convenient place.

All the channels which run rectangular to the wafer plane have twice the depth of the channels parallel to this plane; this arrangement permits a wire to pass the wafer at the bottom or one of the two sides and go to wafers in the same row without leaving its own channel. A sketch of this is shown in Fig. 4.

A frame of a channel wiring assembly for three rows of wafers is shown in Fig. 5. The individual parts of this frame are cast in epoxy, chemically plated and then electro-copper plated to a suitable depth. This is a very economical process since only the masters are machined in brass and then cast in silicon rubber to form the mold for the epoxy pieces. Fig. 6 shows the brass masters, the silicon rubber molds, the cast epoxy pieces and an assembled, copper plated channel wiring unit.

To evaluate the properties of the transmission lines, channels of different widths and cross-cut patterns were machined in a 65-cm long epoxy piece which was then copper plated. This test arrangement, which is approximately ten times longer than the actual channel wiring assembly, was chosen to increase the accuracy of the measurements. Several types of wires were placed in these channels and measurements were made of the characteristic impedance, loss and crosstalk. These measurements were compared with the measurements in a solid piece of silver-plated brass of the same configuration. No significant difference was found between these two pieces. These test transmission lines are shown in Fig. 7. Crosstalk was measured by placing wires in two adjacent channels as seen in Fig. 8. In a single-cut channel, crosstalk was sufficiently reduced (~55db) such that covering the channels was not necessary; however, in the cross-cut channel, silver epoxy or silver paint was required to cover the channels in order to reduce the crosstalk to a value comparable to that obtained in single-cut uncovered channels. Fig. 9 shows an example of crosstalk measurements over the frequency range from 1.75 to 2.1 kilomegacycles.

The Impedance of an Ideal coaxial line, having a 23-mil O.D. "Teflon"* insulation and an 8-mil diameter conductor, was calculated to be 45 ohms using 2.0 as the dielectric constant of "Teflon". In the uncovered line, the inductance will be higher, and the effective k of the dielectric will be lower due to the uncovered top portion of the line. Using the measured k of 1.67, the calculated impedance is 56 ohms as compared to the measured Impedance of 53 ohms. When the line is covered with conductive silver epoxy, the effective

* A registered trademark of the E.I. DuPont Co.
k is 7.5% lower than the value of 2, resulting in a calculated impedance of 46.6 ohms. This compares favorably to the measured value of 46.4 ohms.

In calculating the losses in the coaxial line for this condition, it was assumed that the top half of the outer conductor was covered with silver paint and the bottom half of the outside conductor was copper. Using this assumption, the losses in the epoxy line covered with silver epoxy should be 1.66 times more than the uncovered case, which were measured at 1 and 2 kilomicrocycles to 0.51 and 0.77 db/ft, respectively. These calculations were made using a value of $30 \times 10^{-4} \text{ ohm/cm}$ as the resistivity of the silver paint and experimental results check the factor of 1.66 closely.

If this value of resistivity is accurate, the losses in the cross-cut lines should be 2.4 times higher than those in the coaxial line. Again the experimental values of loss in the cross-cut lines covered with silver paint are approximately 2.4 times the calculated values of a coaxial line.

Insertion loss was measured by plotting points on a Smith chart corresponding to a minimum position on the slotted line and a VSWR reading determined by moving a variable reactance in series with the line in test. Fig. 10 shows the test setup. This method finds the essential insertion loss which is unique for the line being tested. The insertion loss for the line being tested depends on the type of measuring line used. This particular method ignores the reflections at connectors along the line, Therefore, the essential insertion loss, which should be a smooth line as a function of frequency, is slightly less than the actual insertion loss if found by the substitution method. This method also assumes that the variable reactance is lossless. Calculations show that at 1 kmc, the loss in the variable reactance is 0.69 db. When a sufficient number of points are located, a circle can be drawn through the points. This circle can now be rotated so that it lies with its center on the resistance axis of the Smith chart. The equivalent VSWR can be calculated by finding the two values of VSWR at the points where the circle crosses the real axis. If the circle contains the origin of the Smith chart, the equivalent VSWR is found by:

$$\text{VSWR}_{eq} = \left[ \frac{(\text{VSWR}_2)}{(\text{VSWR}_1)} \right]^{1/2}$$

If the circle lies outside the origin of the Smith chart, the equivalent VSWR is found by:

$$\text{VSWR}_{eq} = \left[ \frac{(\text{VSWR}_2)}{(\text{VSWR}_1)} \right]^{1/2}$$

After the VSWR is found, the loss can be found by:

$$\text{db} = 10 \log \frac{\text{VSWR} + 1}{\text{VSWR} - 1}$$

Figure 11 shows a Smith chart with the losses calculated using the above described method,*

*This method was first conceived by D.R. Crosby and makes loss measurements possible without knowing the disturbing influence of connector cables and fittings.

Using a 23-mil wide channel and varying the ratio of conductor to insulator, impedances ranging from 140 ohms to 20 ohms were measured.

The upper limit of characteristic impedance was found by running a 2-mil conductor through a 23-mil outer diameter sleeve of "Teflon". The lower limit was obtained with a 22-mil conductor having approximately a 1-mil coating of "Teflon".

A line with a characteristic impedance of approximately 1 ohm was also built. This line was not a wire as such but a strip of ceramic with a dielectric constant in the vicinity of $k \approx 4000$; it was 10-mils thick, 75-mils wide and 6 to 8-cm long. The high-k material was covered with conductive material on both sides (Fig. 12). This line is intended to be placed in a 75-mil wide channel (Fig. 13). Since the high-k material is very brittle and cannot be bent, its use will be confined to a row of wafers in the channel wiring assembly where the same termination point must be parallel connected to a low-impedance transmission source.

MEMORY CIRCUITS

The packaging requirements of a tunnel diode memory are in some respects more severe, and in other respects easier, than the logic wiring. The easy aspect is that the geometry of each memory plane is fixed and rigid so that the random wiring capability of the logic section is not required. The complication arises from the relative complexity of the basic storage circuit and from the limit placed on the propagation delay due to the high-speed operation, which in our case requires that a 32 by 32-bit memory plane does not exceed a volume of 3.5 inches x 3.5 inches x 0.1 inch.

As to be expected in the construction of a high-speed memory of this type, it is necessary that the bit and word lines must be transmission lines and that ground current paths must be carefully considered. The remaining part of the physical construction is influenced largely by the size of the components and electrical operation of the storage circuit.

We have been concerned with two different storage schemes; one is bit-organized storage and the other is word-organized storage, as shown in Figures 14 and 15, respectively.

The memory plane construction for the bit-organized storage, shown in Fig. 14, consists of metalized alumina sheets which are fired together. The bottom layer is metallized to form a ground plane on one side and 32 tapered lines are deposited on the top side.

The next layer has cut out slots to provide access to the bottom plane. Only its top is metallized. The third layer is also slotted; its top is metallized to form 32 tapered conductors.

After the three layers are registered together and fired, a 30-mil thick single-homogeneous plane is achieved. The slots give access to the 32 transmission lines on the bottom layer.

The next layer is a molded epoxy piece which is 100-mils thick. It is metallized on its top and has 1024
cut outs, one for each storage bit. The round portions of the cut out hold the two resistors which are required for this storage circuit. One resistor is physically longer than the other, but both have the same resistance value. The longer resistor is connected to the transmission line on the bottom layer and the short one to the transmission line which is on the top of the third layer. The tunnel diode is soldered with its anode to the tops of the two resistors and with its cathode to the metallized top of the epoxy piece. Another alumina sheet, metallized on its top, is placed over the anode leads of the tunnel diodes. It acts as a coupling capacitor for all storage circuits and connects to the sense amplifier. Since it is known which bit is interrogated, there is no problem of identification when an output pulse appears. An exploded view of this construction is shown in Fig. 16.

Another type of construction was chosen for the word-organized storage scheme (Fig. 15). While it has the same number of components for each storage bit as the first one, it differs by the requirement that it must be connected to a power supply bus, and that this bus must have the characteristic of a low-impedance transmission line.

A slab of copper-laminated “Teflon” was milled to produce 32 bit lines, each with an unloaded characteristic impedance of 65 ohms. The “Teflon” is 0.020-inch thick and the width of each line is 0.010 inch. The lines are on 0.100-inch centers as shown in Fig. 17. Notched copper bars, 0.010-inch thick, bridge each of the bit lines and permit a common ground at each storage bin. A 0.050-inch wide copper-laminated mylar strip is soldered to each side of the bar. With 1-mil mylar insulation, a characteristic impedance of 2.5 ohms is obtained. One of these lines is the word line, the other serves as a low-impedance supply bus (Fig. 18). The full view of the memory plane with its three lines is shown in Fig. 19.

A molded epoxy stick holds in position the 96 components required for 32 bits and is used as a subassembly as seen in Fig. 20. It is placed between the word lines. The cathodes of the tunnel rectifiers are soldered to the bit lines, the cathodes of the tunnel diodes to the word lines and each resistor is soldered to the supply bus with a jumper.

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Figure 1. Alumina Wafer

Figure 2. Dual Locked-Pair Circuit on Wafer
Figure 3. Wafer Test Jig

Figure 4. Wafer Interconnection With Transmission Lines
Figure 5. Channel Wiring Assembly With Two Wafers

Figure 6. Brass Masters, Rubber Modes, Epoxy Pieces and Assembled Copper-Plated Channel Wiring Assembly
Figure 7. Transmission Test Lines

Figure 8. Part of Test Transmission Line for Double-Cut Channel Crosstalk Measurements
CROSSTALK BELOW -60 db WAS NOT QUANTITATIVELY MEASURED
LINE COVERED OPEN OR SHORT
LINE UNCOVERED AND SHORTED
LINE UNCOVERED AND OPEN

Figure 9  CROSSTALK VS. FREQUENCY OF COVERED AND UNCOVERED TRANSMISSION LINES

Figure 10  TEST SET UP FOR INSERTION LOSS MEASUREMENTS
Figure 11.

ESSENTIAL INSERTION LOSS

VSWR = \left(\frac{5.6}{10.4}\right)^2 = 7.63

\text{db} = 10 \log_{10} \left(\frac{8.63}{6.63}\right) = 10 (0.114) = 1.14 \text{ db}
Figure 12 CERAMIC TRANSMISSION LINE

Figure 13 CERAMIC TRANSMISSION LINE IN THE CHANNEL WIRING ASSEMBLY
Figure 14 BIT-ORGANIZED MEMORY CELL

Figure 15 WORD-ORGANIZED MEMORY CELL
Figure 16  EXPLODED VIEW OF MEMORY CONSTRUCTION FOR THE SINGLE TUNNEL DIODE MEMORY CIRCUIT
Figure 17. "Bit" Transmission Line of Memory Plane

Figure 18. "Word" and "Supply Bus" Transmission Lines Bridge the "Bit" Transmission Lines
Figure 19 32 BY 32-BIT MEMORY PLANE WITH ITS THREE TRANSMISSION LINES

Figure 20 COMPONENTS SUBASSEMBLY FOR 32 BITS