INTERCONNECTION TECHNIQUES FOR SEMICONDUCTOR NETWORKS

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The semiconductor miniaturization approaches which have been described recently have promised complete electronic equipments of extremely small size, light in weight, and of high reliability. Although complete equipments have not yet been built from these devices, this paper will describe some of the factors which must be considered in equipment design and show one technique which might be used for high density equipment.

A typical unprotected semiconductor network is shown in Figure 1. This device is a flip-flop with sufficient gating to permit its use as a counter, shift register or set-reset flip-flop. In this design, two transistors are formed on square mesas near the center of the silicon bar. The material between the transistors forms the collector load resistors. The upper pair of arms extending from the center area are the cross coupling resistors, while mesa areas on these resistors provide the speed-up capacitors. The lower pair of arms is used as resistors on the gating networks. The four diodes required for gating are located along the lower edge of the bar. Two capacitors are formed on a separate bar, using the silicon oxide technique. Thermo compression bonded leads are used to make connections between areas on the upper surface of the bar and for some of the external connections.

In order to be useful, this device must be packaged to provide complete mechanical and environmental protection. The package must also include means for bringing electrical connections in and out of the device and some provision for removing heat from the device. The methods chosen to achieve these results will directly affect the interconnection of semiconductor networks to form complete equipments.

The interconnection technique to be used in end equipment is ultimately determined by the equipment designer. Only he can determine the relative weights to be ascribed to the important factors of size and weight, cost, maintainability and reliability. Different weights of these factors have resulted in very different assembly techniques for radios, airborne computers, and hearing aids, for example. It is not likely that an universal technique will be developed to satisfy these widely different end objectives. This paper will describe a design where size and weight have been minimized at the expense of increased cost.

At some time in the future, it may be possible to fabricate entire equipments, or very large sections of equipments as a single unitary structure. This approach may be considered if self-organizing systems which can tolerate large numbers of defective components can be devised, or if processing yields can be raised to a point very near perfection. At present, however, it is essential to build small groups of components which can be assembled to form the complete equipment.

Although no exact figures exist, it is believed that the optimum complexity for the individual package is a single functional circuit such as a flip-flop, logic element or a gate. Selection of a functional block of this type permits performance testing of the finished unit, which is always desirable and sometimes essential. Since not all of the individual components can be isolated for testing. The flip-flop shown in Figure 1 is near the upper limit for present circuit complexity. This package contains the equivalent of sixteen components.

The use of a package of uniform size makes it possible to connect the packages together with less wasted space between packages, although some space inside the packages is unused. For this reason, all of the digital networks which have been made to date have been packaged in the case shown in Figure 2. The size of this package has been chosen rather arbitrarily. Its rectangular shape permits ten leads to be brought out on the two long sides with a spacing of 0.047 inches. A flat shape was chosen to permit optimum heat transfer from the silicon wafer to the outside of the case.

This package is assembled by the process shown in Figure 3. This process provides a complete glass-to-metal hermetic seal, which is believed to be essential for full protection of the device under severe military environments. Because of the very small mass of the package, it is not susceptible to mechanical shock.

The thinness of the package makes it possible to connect packages together either by stacking or by the use of flat layouts on an etched circuit board. Since the thickness of the package is about equal to that of the common circuit boards, the volumetric efficiency of this technique is quite low. It does offer good
access to the packages for testing and maintenance and should be quite useful in designs where minimum size is not a requirement.

For either the stacked configuration or the flat version, some form of multiplane wiring is probably essential. It is not possible to specify the lead sequence from the packages since the leads must be connected inside the packages to the device as directly as possible. The external wiring must therefore have some provision for crossovers.

One multiplane wiring scheme which has been used with success is shown in Figure 4. Here the packages are stacked, and thin sheets of teflon with metal cladding are used to form the conductors. It is frequently desirable to separate the supply voltage wiring, which may be connected to all packages in a stack, from the signal paths which go from package to package. One sheet may be used for each supply voltage. These sheets are formed with a grid pattern of conductors and holes. The first sheet is placed with the leads of the stack and the leads to be connected to the sheet are bent over and soldered to the sheet. Electrical and mechanical clearances are provided so that the other leads will pass straight through the sheet and will be insulated from it. A second sheet may then be added and connected. Some of the stacks which have been built have used four supply voltage sheets. The signal paths which are required are then formed on similar etched sheets which complete the remaining connections.

An alternate type of construction is shown in Figure 5. The teflon sheets are quite similar to those used in the original version, but small flaps have been cut which can be bent to lie parallel to the leads with which they are to be connected. This version is particularly adaptable to welding. It has the added advantage that no bending of the leads is required and that all leads are available for use as test points after the stack has been connected.

Although defective packages have been replaced in stacks of this type, it would certainly not be attempted for field repair. The stack itself should be considered as the basic replaceable item. Although there is no single figure for optimum throwaway cost for present day military equipments, several studies have shown that the optimum is probably in the range of $200 to $500. It is believed that the cost of a ten to twelve package stack of networks will be within this range for production quantities of devices.

Since the stack is to form the replaceable element, it should be sturdy enough to withstand handling. It should also include a connector to permit easy replacement and isolation of the individual stacks for testing. One such arrangement which has been used is shown in Figure 6. An aluminum frame is used to hold the packages. The teflon sheets are used to provide connections between the packages. The ends of these sheets are then formed around the ends of the frames to provide the male portion of a connector. Flat side plates of aluminum are used on the frame to permit heat transfer from the stack. If required, aluminum foil strips may be placed between the packages and brought over to these plates to further reduce the temperature drop between the frames and the device junctions.

Stacks of this type which will accommodate twelve packages are 0.312 x 0.600 x 0.200 inches. Connections between stacks are provided by strips of connectors, which utilize a similar multiplane wiring scheme. A row of ten stacks is shown in Figure 7. The individual frame side plates are exposed so that the row can be sandwiched between thermal conductors. The edges of the multiplane wiring are again wrapped around an exposed edge of the strip to provide connections between rows.

These rows may then be plugged in to form large sections of an equipment or complete equipments, as illustrated in Figure 8. Multiplane wiring is used between the connector clips.

An assembly of 600 network packages is shown in the photograph of Figure 9. Although the finished equipment is to contain only 600 networks, a 20 per cent overage has been provided, or 720 possible package locations. These have been provided in six rows of ten stacks. Three rows are visible in the photograph, with the other three on the bottom of the package. Thermal mock-ups of the assembly have been completed and the preliminary data will be presented at the meeting.

The size of the finished unit is almost exactly that of a package of regular cigarettes. It would contain about 5,500 individual components in the 600 packages. Total volume required is slightly under 6 cubic inches, including that required for the case, internal heat transfer provisions, and connectors.

This design is not believed to represent the smallest, or the lightest, or the cheapest version possible for this equipment. Many different arrangements of these parts are possible, and some of them may well be more desirable. Different objectives, in particular, may suggest radically different methods of construction. The real significance of this design is that of an existence theorem -- that it is possible to construct useful equipments from systems of elements which are orders of magnitude smaller than existing equipments.
Layout of Bistable Multivibrator (Type 502)
SOLID CIRCUIT semiconductor network

Figure 1 - Layout of Bistable Multivibrator (Type 502)
SOLID CIRCUIT Semiconductor Network
Figure 2 - Outline Dimensions, Hermetically Sealed SOLID CIRCUIT Semiconductor Network

Figure 3 - Semiconductor Network Hermetically Sealed Package Assembly
PACKAGE INTERCONNECTION

STACK OF SEMICONDUCTOR NETWORKS

ETCHED SHEETS IN PLACE

ETCHED COPPER-CLAD TEFLOM SHEETS (SEPARATED FOR CLARITY)

VOLTAGE SUPPLY SHEETS

SIGNAL SHEET

SOLID CIRCUIT semiconductor networks

Figure 4 - Package Interconnection
Figure 5 - Semiconductor Network Interconnection
Figure 6 - Semiconductor Network Stack

Figure 7 - Semiconductor Network Row
Figure 8 - Semiconductor Network Equipment Assembly

Figure 9 - 600 Network Assembly

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