CHARACTERISTICS OF A MULTIPLE MAGNETIC PLANE THIN FILM MEMORY DEVICE

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Summary

In a previous paper,1 a ferromagnetic film memory was described having a complex structure of evaporated magnetic, dielectric and conducting materials. The multiple plane geometry was designed to enhance the characteristics which are desirable in practical digital computer memories without requiring extreme uniformity and control of the magnetic properties.

This paper describes the electrical characteristics of prototype memory elements, and discusses their application in computer memory systems. A short review of the basic magnetic structure and mode of operation is given first to provide a common reference for discussion.

Magnetic Structure and Mode of Operation

The structure to accomplish the selection and storage functions within the matrix is comprised of four ferromagnetic films appropriately interlaced with evaporated drive and read-out conductors, and insulators. All nineteen layers (Figure 1) are vacuum deposited. Figure 2 represents schematically the reference (binary 1) state of the four magnetic layers. The dimensional ratios are shown highly exaggerated for clarity.

The four-layer magnetic complex is in a high or low magnetostatic energy state depending on the sense of M vectors within the films. The low energy, statically stable states are those in which two M vectors point in a direction opposite to the remaining two. Any other configuration results in an unstable high energy state which quickly decays to a stable condition. The difference in film widths causes this decay to proceed by a path involving least expenditure of energy. Due to the difference in the volumes of magnetic material, this minimum-energy transition occurs by reversal of the uppermost film available for reversal. This is illustrated in Figure 8. In going from the "1a" state to either of the "1b" states, the uppermost film available for reversal is the third layer. The fourth (read-out) film thus remains in the original direction and no voltage is induced in the sense conductors. It is seen that any subsequent pulses applied to either X or Y merely affects the first two layers; only coincident drives on X and Y can establish either the "0a" or "0b" states.

Electrical Characteristics

Of primary interest in memory applications are the switching characteristics and the selection ratio of the basic memory cell. Also, in the case of evaporated memories, RLC parameters are of added importance because of the extremely small dimensions attainable. These are now given for the prototype elements.

Resistances of the conductors of prototype elements are centered around two ohms per element. Inductances are in the millimicrohenry range, and capacitances between conductors range from 80 up to 200 microfarads per element. The magnitudes of resistance and capacitance pose some problems in designing an optimum practical array, as discussed later.

To obtain the switching characteristics, pulse sources of variable amplitude and polarity are applied to the X and Y drive conductors connected in series, as shown in Figure 5. The peak output voltage and switching time (measured between 10 percent points) is plotted against current pulse amplitude in Figure 4. The "disturbed 0" outputs normally plotted on graphs of this type are not shown here since it could not be measured with the existing equipment. This is discussed further under selection ratio tests. The rise time of the driving pulse is 20 μs throughout the entire range of currents. The leveling-off effect of switching time at high currents can be ascribed partly to the finite current rise time. This was checked by using a mercury relay pulser with 1 μs rise time and a traveling wave scope. At a maximum current of 3 amperes, the limit of the pulser, the switching time observed was 10 μs shorter than shown in the plot of Figure 4. The switching times below 1.2 amperes are identical with the values of Figure 4, showing that switching time is amplitude limited below 1.2 amperes for 20 μs current rise time. The relay pulser was not used to plot Figure 4 for the reason that a high-current transistor driver capable of rise times below 20 μs do not appear practical at this time. On the other hand, rise times significantly greater than 20 μs would begin to hinder the inherent speed capacity of the device. The figure of 20 μs was thus chosen as the best compromise.

In the low current region, switching can be

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...detected at currents as low as 160 ma, if sufficient pulse width (0.6 µs) is used.

To determine the selection ratio, the circuit of Figure 3 is slightly modified so that the X and Y windings can be driven separately by adding another pair of pulse generators. The X winding is driven by 3 amperes (limit of equipment) rising in 20 µs in the READ direction and 500 ma, in the WRITE (reset) direction. The Y winding is driven with 500 ma, in both directions. The photograph in Figure 4 shows superimposed traces of the output voltages, all during READ time, under three different conditions:

1. Only X is driven in the READ direction followed by a coincident WRITE drive.
2. WRITE drives are removed.
3. Both X and Y are driven coincidently in the READ direction followed by coincident WRITE drives.

The output voltage resulting from the third condition represents a full select "1" and is shown for reference. The second output is the "zero" signal reference since no writing occurs prior to READ, and the output for condition 1 shows the effect of a 3-ampere half-select pulse. The difference in output voltages between condition 2 not during condition 1.

Besides the switching characteristics and selection ratio, another parameter of interest, especially in fast memory systems, is the delay of the output signal in propagating over the sense conductors. The problem is accentuated in the thin film element because the extremely small dimensions result in larger values of capacitance. The delay, with any sequence of disturb pulses. Second, once a 1x or 0x state is entered, it is not possible to return to the reference states. In all cases the fourth layer is magnetically decoupled from the driven layers. Further, once the disturbed states are entered, the two bottom layers are not affected by further disturb pulses. This "decoupling" feature implies a somewhat more subtle writing technique than core memories using inhibit currents for digit control.

Memory organizations based on biasing a winding or adding (or modifying) a conductor (to obtain economy in the driver count) are presently under evaluation. One important consideration in this evaluation is developing an optimum method of interconnecting the elements to obtain cancellation of capacitively coupled noise, analogous to the use of diagonal sense windings in core arrays to cancel inductively induced noise. Another consideration is the effect of the relatively high resistivity of the conductors. If 1R drops are traced in Figure 7, it can be seen that care must be exercised to insure that the voltage drops in
access lines do not cause excessive voltage gra-
dients across the extremely thin insulating
layers.

In applications involving large numbers of
cells a reduced cell length and reduced magnetic
film thickness is used. One of the virtues of
the cell is that, where desirable, thicker films
and longer lengths may be employed to achieve
substantial outputs, such as with the .200" cell
in obtaining all the previous data. However, in
large systems the problems of power dissipation
per cell, back e.m.f. per cell, output signal
delay per cell, and maximum storage density per
surface area dictate the use of a smaller cell.
Smaller size is feasible because of the vacuum
techniques employed, and the use of a reacting
system such as this, where flux may be switched
at any location, becomes practical due to the
minute amounts of magnetic material that can be
employed using vacuum, vapor-phase processes.

Conclusion

The multi-layer memory elements offer con-
siderable promise in application to high speed
memory systems. A number of problems remain to
be solved in designing peripheral circuitry
compatible with the speed capabilities of the
device, and in improving certain characteristics
of the device itself. These are currently under
investigation.

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Reference

E. D. Broadbent, Proceedings 1959 Special
Technical Conference on Nonlinear Magnetics
and Magnetic Amplifiers, September 1959.

Figure 1. Schematic section of an evaporated memory cell.
Figure 2. Schematic representation of the four-plane magnetic system.

Figure 3. Basic test set-up for obtaining switching characteristics.

Figure 4. Switching characteristics.
Figure 6. Delay measurements.

Figure 7. Simplified representation of a possible memory organization.

Figure 8. Possible H-vector configurations.