UNIFLUXOR: A PERMANENT MEMORY ELEMENT

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Introduction

The Unifluxor is a new binary permanent memory element which appears to have the advantages of high-speed operation, easy fabrication, and low cost. Unlike cores, twistors, capacitors, and other commonly used memory devices, the Unifluxor does not depend upon the hysteretic properties of some nonlinear material but instead uses the inductive characteristics of magnetically coupled wires.

A Unifluxor memory array consists of a printed-circuit board upon which are etched longitudinal drive lines and transverse sense lines. Each intersection of a drive and sense line represents one bit, with the bits of one word lying along the same drive line. Thus the array operates in the word-organized mode.

The particular state of each bit depends upon the presence ("one") or absence ("zero") of a copper slug. The copper slugs, properly spaced and oriented, are contained on a plastic film cemented in place over the printed-circuit board (Figure 1). In order to change the contents of the memory, it is necessary to substitute a new cover film with the desired pattern of copper slugs.

Theorem of Operation

"Zero" State

Consider a wire in the plane of and perpendicular to a closed wire loop (Figure 2). When the switch is closed and current flows in the wire, a cylindrical magnetostatic field is created around the wire, the effective boundary of which is indicated in the diagram by dotted lines. The total flux within the loop then is \( \Phi_1 + \Phi_2 \).

At the time the switch is closed and the field is building up, an emf (E) is induced in the loop according to Faraday's equation:

\[
E = -N \frac{d\Phi}{dt}
\]

Since \( \Phi \) is equal to the product of the flux density (B) and flux area (A), equation 1 may be rewritten as:

\[
E = -N \left( \frac{d(B_1 A_1)}{dt} + \frac{d(B_2 A_2)}{dt} \right)
\]

For the case illustrated, the following equalities exist:

\[ B_1 = -B_2 \]
\[ A_1 = A_2 \]

Thus, the emf's generated in the two halves of the loop are equal in magnitude but opposite in sign, and the net output is zero. This in fact is the condition for a Unifluxor in the "zero" state where the loop is the sense line, the wire the drive line, and the switch the logic which selects the particular drive line.

"One" State

Consider a second loop-and-wire arrangement similar to the first (Figure 3). Here, however, a copper slug has been placed in the path of \( \Phi_2 \). At the time the switch is closed and the field is building up, Eddy currents and other losses (depending upon the configuration) are induced in the slug. The effect of the losses is to reduce \( B_2 \) such that:

\[ B'_2 = B_2 - \Delta B_2 \]

If the new value \( B'_2 \) is substituted in equation 2, it becomes evident that a net emf proportional to \( \Delta B_2 \) will be induced in the loop and a signal will appear at the output transformer. A similar signal but opposite in sign will appear when the switch is opened and the field collapses. This is the condition for a Unifluxor in the "one" state.

Design Considerations

The amplitude of the "one" signal depends upon:

1. The rate of change of the current in the drive line;
2. The final amplitude of the current;
3. The spacing between the two legs of the sense line loop, and
4. The amount of flux imbalance introduced by the copper slug.

Each of these parameters influences the design of an operating memory. General considerations are discussed below, followed by values of the parameters chosen for a working model of the Unifluxor memory.

The need for a rapid build-up of a current limits the length of the drive line, since as the line is made longer its inductance becomes larger and hence objectionable. The desired cycle time also influences to a smaller degree the maximum allowable length.
The final amplitude of the current determines the effective boundary of the flux of the drive line, that is, the point at which \( B_{(\text{max})} \) is essentially zero. The drive lines adjacent to the selected line must fall outside this boundary; otherwise noise will occur whenever the drive line on one side of the selected line has a slug and the line on the other side does not. The amplitude of the current thus determines the minimum spacing between drive lines.

The position of the effective boundary of the drive line field is one factor in determining the flux area; the second factor is the spacing between the legs of the sense line loop. In order to obtain an area of sufficient size and consequently a "one" signal of reasonable strength, a compromise must be reached between current amplitude and the spacing of the loop. For a very small current, if the drive lines are close together, the sense line legs must be widely spaced, thereby keeping the over-all size of the array relatively constant.

The amount of flux imbalance caused by the slug is determined by its position, size, and shape. Theoretically, an open slug which completely cancelled the flux in area \( A_0 \) would cause a maximum \( \Delta B_2 \), the decrease resulting not only from Eddy current losses but also from the field of the counter-emf that would be induced in the loop. In practice, a solid rectangular slug is sufficient, yielding a strong "one" signal with excellent signal-to-noise ratio.

**Working Model**

**Physical Arrangement**

A working model of the Unifluxor memory has been constructed for experimental purposes. The memory has a capacity of 64 words of 50 bits each. The 64 words are contained on two arrays of 32 words each. The drive lines of the two arrays are shared in common; the sense lines are independent. The configuration of the memory element used in the model is shown in Figure 4, which is an enlarged diagram of several bits.

Note that the sense line crosses the drive line at an angle. The adjacent drive lines are crossed at the same angle but in the opposite direction. Skewing the sense lines in this way serves two purposes: It permits the slug to be so placed as to interrupt \( B_2 \) in two areas, thus achieving more imbalance, and in addition it tends to cancel any noise originating from nonselected drive lines.

To read any given word requires full current on the selected drive line and no current in the other drive lines. The selection must be near perfect, else each leakage current will cause small outputs from the "one" bits through which it passes. This noise, multiplied by the number of drive lines linked by the same sense line, can reduce the signal-to-noise ratio and mask the selected bit.

One way of obtaining perfect selection is to use a separate driver for each bit. The economic obstacle this method imposes, however, obviates its use in a large memory. For the laboratory model a switch-core selection system was chosen which involves four drivers, eight gates, and 32 switch cores. Each switch core selects two drive lines, one on each of the independent arrays. The outputs from the two corresponding sense lines appear at gates at the input to the sense amplifier. The gates permit the output from only one sense line to pass at any one time.

Two different sense amplifiers have been designed. One amplifier produces an output whenever any negative-going pulse appears at its input. No output is produced for positive-going inputs. The second amplifier produces an output only if the leading pulse is negative, with no output under other conditions. Both amplifiers have extremely fast recovery times.

A full discussion of the address logic is omitted from this paper, since the logic is similar to many other addressing schemes for word-organized memories. However, a novel method of selecting the drive cores has been devised, which reduces the noise level far below that usually experienced.

The principle is illustrated in Figure 5. In quiescent state, the address translator holds the driver and gates cut off. (The full schematic of only one gate is shown, the circuits of the others being identical.) No current flows through the core winding associated with gate 1 because of the blocking action of the diode. So also for the other two core windings: No current flows.

Assume that the driver and gate 1 are now simultaneously enabled, as indicated by the small waveforms on the diagram. A low-resistance path from ground is created through Q1 through the winding of the left-hand core, through Q2 to the positive side of the supply. The magnitude of the current through the winding is sufficient to select the core, and an output pulse appears on drive line 1. No current flows in the nonselected core windings because gates 2 and 3 remain closed.

Although it would appear possible theoretically to eliminate the drive core and let Q1 drive the drive lines directly, in practice this causes ringing on the drive line.

**Electrical Characteristics**

A 500-milliampere pulse 150 millimicroseconds wide is used as the drive current. The flux created by the current at its maximum has a density of approximately one gauss at a distance one millimeter from the drive wire, as calculated from the equation:

\[
B_{(\text{gauss})} = \mu I 10^4/2\pi R \theta
\]

This equation considers the drive line as infinitely long, an assumption justified by the ratio of its actual length to the diameter of the effective field. The value of \( \mu \) may be taken as that for free space \((4\pi 10^{-7})\). \( \theta \) is a unit vector normal to the drive line.
The net emf induced in the sense line by a "one" bit has a range of 8 to 12 millivolts. The corresponding output from the sense amplifier is a rise from -4 volts to 0 volts. Figure 6 shows the sense amplifier outputs for both "one" and "zero". The signal-to-noise ratio is greater than 15 to 1.

At present, the memory is being operated at interrogation intervals of 420 millimicroseconds. An interval of 350 millimicroseconds appears possible with the present design. The maximum possible interrogation rate of the memory element itself is not known, the recovery time of the sense amplifiers and the speed of the address logic being the limiting factors in the present design. No heating or other adverse effects have been noted from repeated interrogation of the same drive line.

Fabrication

The drive lines are etched on an epoxy glass substrate and made flush with the surface by heating the substrate to 375°F and placing it in a 50-ton press. A Mylar film with a copper sheet bonded to it is cemented in place on the substrate, and the sense lines are etched from the copper sheet.

The copper slugs are etched on a second Mylar film, with a slug in each bit position. When the contents of the memory are determined, the slugs in the "zero" positions are punched out and the film cemented to the sense and drive line array.

(For customer use, thin stiff cards appear more desirable as a base for the slugs. A mechanical arrangement which holds the cards firmly in position against the control lines without cement has been developed, and the cards may easily be exchanged. A device to prepare cards with the desired slug arrangement semiautomatically is now being investigated. Using standard punched paper tape as input, the device activates a bank of lamps, exposing photo-resist material on the previously sensitized card. The card is ready for use after development and cleaning.)

None of the fabrication processes are critical or expensive, nor do any require highly skilled operators. In the model built for use in the laboratory, a density of approximately 200 bits per cubic inch was achieved with little effort. The array may further be scaled down by decreasing the distance between drive lines and the width and separation of the sense line loops. (In the laboratory model, these dimensions were made conservatively large.)

Conclusions

The Unifluxor is particularly suited for instruction storage in such fixed-program machines as process control and missile guidance computers. The speed of the element is sufficiently high as to adapt it for use in next-generation machines. Although life tests to prove its reliability have not yet been performed, the element itself does not appear to have any characteristic that would change either with time or operation, and hence the reliability of the memory control circuits would be the governing factor.

Another potential application now being investigated is dictionary storage for machine translation. The low cost of the Unifluxor may make possible random-access memories of a size hitherto unfeasible economically. If the memory element itself was the only aspect of this problem, the Unifluxor would solve it; the cost of the control circuits, however, remains and must first be reduced.
Figure 1. Simplified Diagram of Unifluxor Memory

Figure 2. "Zero" Configuration
Figure 3. "One" Configuration

Figure 4. Enlarged Section of Unifluxor Array
Figure 5. Core Selection

PATTERN 1011 IS THE RESULT OF INTERROGATING FOUR SEPARATE DRIVE LINES IN SUCESSION.

Figure 6. Sense Amplifier Output