A WORD-ORIENTED TRANSISTOR DRIVEN NON-DESTRUCTIVE READOUT MEMORY

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Summary

Using three-aperture ferrite memory cells, a 512-word non-destructive readout memory has been operated with transistor drivers. Writing and reading are both achieved with bipolar two-pulse sequences, which are, respectively, ERASE, WRITE and SET, READ. Due to the inherently non-destructive manner in which the cells are operated, no regeneration cycle is necessary to restore information to interrogated cells. The necessary bipolar writing and reading pulse sequences are conveniently provided by a novel magnetic switch matrix, in which all rows and columns are driven in coincidence except those intersecting at the desired address. The resultant driving current at the desired address is the sum of all the transistor driver currents, or 2(n-1) times the individual transistor driver currents for an "n" square matrix.

Introduction

Since the invention of the ferrite core coincident-current computer memory, there have been several systems advanced to utilize the best features of the coincident-current system while improving upon or circumventing its deficiencies. Many of the alternate methods utilized a multiaperture device fabricated from a square hysteresis-loop type of ferrite as the building block for the memory storage or logical operations performed by the system. Each scheme used the ferrite material's ability to store a flux level or previously ordered flux geometry without a constant power expenditure. The Transfluxor, of Rajchman and Lo, offered proportional output instead of just ONE-ZERO operation, or, if desired, a random-access ferrite core memory with non-destructive readout. The Hunter and Bauer coincidence flux schemes as further improved by Baldwin and Rogers were able to circumvent the coincident-current memory's inherent maximum drive current limitations and achieve improved access and switching times for a memory system. The dc bias offset method as used by Lawrence overcame the necessity of using square hysteresis-loop ferrite material. All of these systems were built upon multiaperture ferrite cells and required driving currents somewhat larger than the coincident-current system. Since the coincident-current system in turn required driving currents on the order of one-half ampere, it was not feasible until recently to utilize solid state devices for driving a memory system. Constantine has shown a load sharing matrix switch which is suitable for some applications.

The memory system described here is also based upon a multiaperture ferrite cell which, superficially, differs little from previous such schemes, either in driving currents or core geometry. This system, however, embodying the multiaperture cell and the novel driving matrix developed for it, offers the prospect of a random-access transistor-driven computer memory with non-destructive readout and access times comparable to a coincident-current system.

The multiaperture memory cell operation will first be described in detail. The novel driving matrix and the memory planes for a system using these cells will then be explained and finally the entire memory system is described.

Multiaperture Memory Cell

The basic memory cell is shown in Figure 1. Cell geometry is important and the dimensions of this cell were fixed largely by compromise between performance, drive requirements, and fabrication ease. Cell performance is a fairly sensitive function of relative hole sizes and spacings (geometry), while drive currents vary inversely to the absolute hole diameters. The smaller the cells, the more difficult they are to fabricate by pressing from unfired ferrite powder. The cell chosen was near the minimum size which could be manufactured in the laboratory without special production techniques.

Every memory cell is normally linked by three windings, one each for Drive, Inhibit and Sense functions. Except for the necessity of noise cancellation in a plane of these memory cells, the Inhibit and Sense operations could both be served by a common winding.

Writing and Reading are each accomplished with a bipolar, two pulse sequence applied to the Drive winding, utilizing driving core output in both drive and reset directions. This allows a maximum simplification of the means connecting driving core and memory cell.
The pulse sequences used are shown in Figure 2. ERASE, READ, WRITE and INHIBIT pulses are typically 0.5 to 1.5 microseconds wide, depending upon clock rate used. SET pulse is typically 1.5 times the width of the READ pulse. READ and WRITE pulses for simplicity are of equal amplitude, typically 1.5 to 2.5 amperes. ERASE and INHIBIT pulses are typically 1.5 to 3.0 amperes. SET pulse magnitude is generally a third to half of the ERASE current. Output voltages are typically 1 to 2 volts, with 0.1 to 0.2 microsecond widths. ONE/ZERO ratios are generally 5/1 to 10/1 for and individual cell.

A ONE is written into the cell by applying to the Drive winding the pulse sequence shown in Figure 2a.

If the cell was previously unmagnetized or was storing a ONE, the cell's flux distribution following the ERASE and WRITE pulses are shown in Figures 3a and 3b respectively. A pulse of either polarity into the Drive winding results in a flux around the center hole only, regardless of magnitude. Although a current through the Drive winding applies a magnetizing force around both the small center and large left-hand holes, the maximum primary magnetic path length around the small hole is less than the minimum magnetic path length around the large hole. As the current pulse increases from zero, the area encircling the small hole is saturated before the mmf applied around the large hole becomes sufficient to overcome the threshold coercivity of the ferrite material. The flux encircling the large hole cannot increase significantly through this saturated region.

Considering the above, it is seen that the ERASE and WRITE pulses result respectively in clockwise and counterclockwise saturation around the small hole as shown in Figures 3a and 3b.

A ZERO is written into the cell by applying an INHIBIT pulse in time coincidence with the WRITE pulse. As before the preceding ERASE pulse would have destroyed any stored information. The flux distribution following the INHIBIT or WRITE ZERO sequence is shown in Figure 3c. Saturation around the outside holes occurs because no net current flows through the center hole and mmf is applied only around the outside holes. This mmf directly opposes the post ERASE saturated flux around the small hole in the leg common to the left-hand hole. The mmf resulting from WRITE and INHIBIT pulses in coincidence therefore destroys the flux encircling the small hole and allows this flux to be redirected around the outside holes.

Readout is accomplished with the bipolar pulse sequence of Figure 2c applied to the Drive winding. To avoid extraneous output signals, stored information is detected by observing the Sense winding output voltage only while the READ pulse is applied to the Drive winding. Changes in flux linking the Sense winding during ERASE, WRITE and SET operations may also induce voltages in the Sense winding. These are, however, ignored and only those Sense winding outputs occurring in synchronism with the READ pulse are relevant to information stored in the cell.

If the interrogated cell stores a ONE, the small SET pulse assures that the flux encircling the center hole will be in such a direction that the following READ pulse will reverse it and induce an output in the Sense winding. Successive READ sequences may repeat this dual reversal as often as desired, resulting in non-destructive readout of a ONE.

If the interrogated cell stores a ZERO, the small SET pulse is of insufficient magnitude to overcome the coercivity of the flux path surrounding the large left-hand hole. The SET pulse leaves the ZERO-storing cell arranged such that the following READ pulse causes no flux change about the center hole and therefore induces no output voltage(ZERO readout) in the Sense winding. Repeated READ sequences also fail to effect flux changes in the cell storing a ZERO, allowing unlimited non-destructive readout.

From the discussion of the READ sequence, the governing factors determining SET pulse parameters will now be apparent. To obtain as fast operation as possible, it is desired to make the SET pulse of high amplitude. As the SET and ERASE pulses are of the same polarity, there is obviously a SET pulse amplitude above which a stored ZERO is destroyed. By reduction of the SET pulse amplitude below the destructive readout threshold, its volt-time area and hence flux reversal capacity has been decreased. The SET pulse is therefore increased in width to switch the majority of flux encircling the small hole of a ONE storing cell.

The erase mechanism may be clarified by the following explanation. If the cell previously stored a ONE, the ERASE pulse has the same effect as a SET pulse, and the resulting flux configuration is as shown in Figure 3a. An ERASE pulse applied to a cell storing a ZERO first reverses the clockwise flux encircling the left-hand hole, since the resulting mmf opposes this flux. This mmf also opposes the flux in the outside leg of the right-hand hole. Once the opposing ERASE mmf is large enough to destroy the fluxes encircling the outside holes, the mmf around the center hole is very intense and the available flux in the center legs is reoriented around the center hole as shown in Figure 3a.
The memory cells are normally arranged in multicell planes or matrices in which all cells are threaded by common Sense and Inhibit windings. Inhibiting is done on a planar basis and the effects of a random INHIBIT pulse on a non-selected cell must be considered. If the cell stored a ONE, the random INHIBIT pulse simply reverses the flux surrounding the center hole, just as a SET pulse would have done, and the stored ONE is unharmed. A READ sequence then applied to a cell in this condition would produce the usual Sense winding ONE output in synchronism with the READ pulse.

A random INHIBIT pulse applied to a cell storing a ZERO produces an mmf in the direction of the saturated flux around the right-hand hole and causes no flux change. It is seen that though the random INHIBIT pulse may cause flux changes in the unselected cells, no adverse effects occur and stored information is not destroyed.

The flux distributions utilized to explain the multiaperture cell's operation have been verified experimentally by integration of the voltages induced in a winding threading one or more holes at a time. By this technique it was possible to observe the net flux about any single hole or through any of the various legs of the cell. Though the flux distributions thus obtained may undoubtedly be explained in other terms, such as those employing crescent-shaped flux patterns, the relatively simple explanation presented here, supported by ample experimental evidence, is felt to be perfectly valid.

Complement Switch Matrix

The bipolar pulses required for the pulse program of the previously described multiaperture memory cell are conveniently supplied by a switch matrix of tape wound cores. To achieve the drive currents desired for high speed operation and still use transistors as the pulse generators, a non-conventional circuit is used. No dc reset current is used, allowing all of the transistor current flowing to be used for switching. In the complement switch matrix to be described, the complement of the row and column address is excited, i.e. all rows and columns except those intersecting the desired core. For example, a 3x3 array is shown in Figure 4 with appropriate drive windings. For simplicity no reset or word drive windings are shown. All cores are initially mangetized clockwise. If it is desired to select core 9, all rows and columns other than row 3 and column 3 are excited at an amplitude I. The excitation received by cores 1, 2, 4 and 5 is equal to the algebraic sum of the magnetomotive forces due to the 4 turn row, 4 turn column and single turn cancel windings. For these cores that is 4I+4I-4I=+4I, clockwise magnetization assumed positive. Thus none of these cores are switched irreversibly. Cores 3, 6, 7 and 8 are excited either by a row or column winding (not both) and the single turn cancel winding. Their excitation is therefore 4I-4I=0. Selected core 9 is driven exclusively by the single turn cancel winding. Core 9 is thus excited by -4I which causes it to switch irreversibly. The effect of this wiring scheme is to permit transistor currents to parallel into a single turn through the selected core.

In a practical system a reset winding is wired to produce clockwise magnetization in every core. In the system to be described, two identical complement switch matrices are used. The cancel winding of one matrix is extended and threaded in reset fashion through the other matrix. The number of turns required for the row or column windings of an "n" square matrix is 2(n-1). Individual word drive lines are associated with each switch core on a core per word basis as shown in Figure 5.

The transistor circuitry associated with the complement switch matrix drivers is shown in Figure 6. Current routing, current mode switching and grounded base switching are used to achieve speed from economical transistors. When either T_3 or T_4 is driven by the excite pulse in the absence of a negate pulse on D, the emitter of T_2 is driven positive with respect to its base and conduction takes place. If a 16x16 complement switch is used, 29 transistors associated with the other rows and columns are driven in like manner. One row and column will be negated for address purposes. On the application of an excitation pulse simultaneously with a negate pulse, diode D conducts turning off T_1 which drives the base of T_2 more positive than its emitter. T_2 therefore will not conduct these conditions. The voltage on the common bus is low due to the conduction of thirty transistors in parallel compared with the voltage developed across the switched core. Independent supply voltages E_1 and E_2 allow control of the pulse amplitudes and durations for two separate excite pulses later to be called ERASE and SET. Though this circuit appears deceptively simple, many subtleties caused other circuits to be rejected in favor of this simple one. Enumeration of some of the more important considerations will be discussed during system description.

Memory Cell Matrix

Figure 7 illustrates a 3x3 memory plane wiring scheme for non-destructive readout of multiaperture cells showing planar Inhibit and Sense windings. Noise cancellation is used as in conventional memory planes, necessitating a separate inhibit line.
Memory System

Figure 8 shows the block diagram of a test vehicle embodying previously described circuits. In operation one switch matrix is operated in a "selective mode", i.e. it selects the address of the word to be written or read. The other switch matrix is operated in a "non-selective" mode, to reset the selective mode switch matrix. Either of the switch matrices may be used for either mode, but for simplicity SM-1 will be described in the complement selective mode and SM-2 will be chosen for non-selective mode reset. Thus SM-2 will be driven in such a manner that no cores in SM-2 switch by driving all rows and columns; but SM-2's current will switch the previously selected core in SM-1 back to the reset position.

The program shown in Figure 2 will be used for a four pulse sequence of ERASE, WRITE, SET and READ. SM-1 driven selectively generates a large ERASE pulse which clears all memory cells on the addressed word line. The polarity of the ERASE pulse is opposite to the READ and WRITE pulses. This operation is followed by driving SM-2 non-selectively which resets the addressed core of SM-1. A WRITE pulse is generated by this operation which is of sufficient magnitude to write a ONE in all addressed cells. Those planes in which a ZERO rather than a ONE is desired are energized simultaneously with an INHIBIT pulse applied to the memory plane inhibit winding. Both SM-1 and SM-2 are now in the normal state, that is all cores switched to the same sense. Clearly this operation may be followed either by another Write sequence or, as will be shown, by a Read sequence.

The read operation consists of two phases; the SET and READ. SM-1 is driven selectively at an amplitude which will not clear cells in the ZERO state and for a duration sufficient to switch all the cell flux desired. Following the SET pulse, a READ pulse is provided by driving SM-2 non-selectively to reset SM-1. Simultaneously a strobe gate energizes the memory plane sense amplifiers. If a ONE is present in a plane, sufficient output voltage will be generated to excite the sense amplifier. If a ZERO is present, the noise voltage is of insufficient amplitude to energize the sense amplifier. Strobing is necessary to prevent spurious outputs during the other operations.

Governing factors pertaining to the previously described row and column switching circuit may now be considered. It had first been thought that adequate speed and current could be obtained by using a dc source and driving row and column gates in parallel to excite the switch matrix. The required independent control of duration and amplitude for the ERASE and SET pulses, however, make this method very difficult to implement. Another fault of such a scheme is the loading effect caused by the transistor drivers during reset operation. These loading effects may be due to one or all three of the following:

1. Minority carrier storage
2. Output capacitance of the driver circuits
3. Conduction of the driver due to polarity of the induced voltage (such as emitter followers).

In the configuration described, larger output currents result at speeds not possible in the dc collector supply type of operation. Further, the polarity of the induced voltage during reset aids turn off by negatively biasing the emitter of T2 in Figure 3. The adjustment of SET pulse amplitude may be performed in a single stage by a simple change of dc level. Negation of a row and column is independent of the applied ERASE and SET pulse amplitudes and durations, greatly simplifying the system.

In the test vehicle shown, although random access is allowable, the test program used provides sequential addresses via a shift register for negating one row and column at a time. This greatly aided trouble shooting during "de-bugging".

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References

Figure 1. Dimensions and windings for a typical multiaperture memory cell. Typical thickness is about 0.045 inches.

Figure 2a. Bipolar current pulse sequence applied to Drive winding for storing either a ONE or a ZERO.

Figure 2b. Current pulse applied to Inhibit winding for inhibiting or writing a ZERO.

Figure 2c. Bipolar READ sequence for interrogating multiaperture cell.

Figure 2d. Typical ONE readout voltage from interrogated cell, showing coincidence of readout and READ pulses.

Figure 3a. Flux distribution resulting from application of ERASE pulse to a cell storing a ONE.

Figure 3b. Flux distribution resulting from WRITE pulse. The cell is now storing a ONE.

Figure 3c. Flux distribution resulting from INHIBIT or WRITE ONE sequences. The cell is now storing a ZERO.
Figure 4a. Complement switch matrix.

\[ +4I \quad +4I \quad 0 \]
\[ +4I \quad +4I \quad 0 \]
\[ 0 \quad 0 \quad -4I \]

+ = CLOCKWISE INITIAL MAGNETIZATION
- = COUNTERCLOCKWISE SWITCHING DIRECTION

Figure 4b. MMF chart.

Figure 5. Driving core and word line scheme used to drive multiaperture memory cells.

Figure 6. Transistor circuitry for driving switch matrix.
Figure 7. Typical memory cell matrix with planar Inhibit and Readout or Sense windings.

Figure 8. Test vehicle for system utilizing multiaperture memory cells.