High-Speed Circuit Techniques Utilizing Minority Carrier Storage to Enhance Transient Response

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SINCE the introduction of transistors to the digital computer field, many circuit techniques have been employed to mechanize computer logic, flip-flops, and in general, bilevel switching operations. Initial transistor applications to digital computers employed circuit techniques carried over from vacuum-tube computer technology and in many instances the vacuum tube has been replaced; base for grid, emitter for cathode, and collector for plate, with the configuration of the other components of the circuit remaining unchanged.

Because the transistor is basically a current amplifying device rather than a voltage amplifier like the vacuum tube, modifications in switching circuit techniques have continuously evolved to minimize undesirable characteristics of the transistor or, more fully, to employ its inherent characteristics. Notable examples of such evolution, which depart radically from techniques used in vacuum-tube switching circuits, include transistor antisaturation techniques, direct-coupled transistor logic (DCTL), current mode gating, and transistor avalanche circuit techniques.

This paper describes still another approach to semiconductor digital-computer switching circuits. Here the normally undesired minority carrier storage effects of high-conductance silicon junction diodes are utilized in combination with transistors to produce very fast transient response in flip-flop and pulse circuits.

Minority Carrier Storage in Diodes

The minority carrier storage effect exhibited by junction diodes is well described in the literature. This storage effect is illustrated in Fig. 1 by the voltage and current wave forms for a junction diode being switched from forward to reverse condition. In this illustration, the diode $D_1$ is driven by a constant current source in the forward direction and by a constant voltage source in the reverse direction. Reverse current is limited by the series resistance $R_I$. Diode $D_2$ decouples $R_I$ from the circuit during the reverse half-cycle so that all stored charge in $D_1$ is discharged through $R_I$.

The wave forms of Fig. 1 may best be understood by referring to the instantaneous diode volt-ampere characteristic shown in Fig. 2. The forward characteristics are shown in the positive quadrant account for the diode current and voltage wave form when the diode is reversed biased by $E_r$ and the current limited by $R_I$. If it is assumed that diode $D_1$ has no loss, i.e., no forward voltage drop, the saturation reverse current will be given approximately by

$$I_s = \frac{E_r + E_{2r}}{R_I}$$

where $E_{2r}$ is the reverse saturation voltage (obtained from the instantaneous volt-ampere characteristic of the diode). If the resistance of $R_I$ is reduced to a value $R_I'$ the current-voltage wave forms for the diode will appear as Fig. 3. The reverse saturation current will increase as noted. As $R_I$ is reduced still further, the reverse saturation characteristics eventually will not be observed, unless the current in the forward half-cycle is increased. The total charge delivered through the load resistor $R_I'$ will be approximately the same as in Fig. 1, provided that the time interval under consideration is short in comparison to the lifetime of the carriers, i.e., recombination of carriers need not be considered. If the value of $R_I$ is reduced, thus increasing the diode forward current, the total charge $Q_s$ stored in the diode by minority carriers will increase and, in fact, for a given diode, $Q_s$ will be a function of both the magnitude of forward current and its duration. It should be noted that the instantaneous reverse characteristics indicated for the diode are very similar to typical transistor characteristics. Excess stored minority carriers in the diode under reverse conditions act exactly as excess carriers injected by the emitter of a transistor. Since there is no emitter current, the reverse characteristic of a diode is, of necessity, instantaneous. Techniques have been described in which these characteristics may be employed to provide a diode amplifier with both current and voltage gain.

Having described briefly the diode characteristics of importance for purposes of this paper, attention is now given to a number of semiconductor switching, gating, and pulse circuit applications which employ these characteristics to provide efficient and fast transient performance.

Storage-Diode Coupled Flip-Flop

Factors of prime importance in the design of fast-response transistorized flip-flop trigger circuits include; turn-on time $t_6$, storage time $t_8$, and turn-off time $t_9$. Total transient response time for a triggered flip-flop may be defined as the time required for the flip-flop, consisting of two cross-coupled amplifiers, $A$ and $B$, to change from a steady state condition no. 1, i.e., amplifier $A$ conducting and amplifier $B$ cut-off, upon application of a trigger pulse, to a steady-state condition no. 2, i.e., amplifier $A$ cut-off and amplifier $B$ conducting. Here, all three delay times, $t_6$, $t_8$, and $t_9$ are involved. A reduc-

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tion of one or more of these time intervals will reduce the over-all transient response
time.

Fig. 4 shows the schematic diagram of a base-triggered flip-flop circuit utilizing
the storage diode cross-coupling tech-
ique to reduce delay times \( t_1 \) and \( t_2 \). The
turn-on time \( t_b \) of the triggered transistor, i.e., the initially "off" transistor, is re-
duced by a similar technique which is de-
scribed later. In all cases, the end re-
sult using a storage diode will be to pro-
vide "over drive" for the base of the

Fig. 1. Response of a silicon junction diode switched from forward to reverse bias

Fig. 2 (left). Instantaneous volt-ampere characteristic of a diode switched from forward to reverse

junction with conducting clamp diode
\( D_b \). The collector of \( T_1 \) will be a poten-
tial of approximately \(-1.5\) volts, a level
established by the sum of forward drops
in conducting diode \( D_0 \), a silicon storage
diode, and the base-emitter junction of
transistor \( T_2 \). The current through \( D_0 \)
will be the sum of the base current of
\( T_2 \) plus the current \( i_{bb2} \) through the back bias
resistor \( R_4 \). Minority carriers will have
been injected and stored in both diode
\( D_0 \) and the base region of transistor
\( T_2 \). The voltage at the base of
\( T_2 \) will be approxi-
ately \(-0.5\) volt established by the
base characteristic of \( T_2 \); therefore, the
base clamp diode, \( D_6 \), is in a noncon-
ducting state. Transistor \( T_2 \) thus will be
held in saturation so that its collector volt-
age \( e_c \) will be approximately \(-0.1\) volt
for the transistor and current levels
chosen. The voltage across storage diode

Fig. 3. Effect of lowering resistance in reverse diode dis-
charge circuit and in forward charge circuit

Fig. 4. Storage diode-coupled flip-flop

Retzinger—High-Speed Circuit Techniques
D1 is approximately 0.35 volt, a value below the forward conduction threshold for a silicon diode. Steady-state d-c stability for the circuit shown thus is assured.

Referring now to the wave forms of Fig. 5, trigger action of this circuit may be explained. Upon application of a negative current pulse of sufficient amplitude to the base of T2, the collector of this transistor will be driven to a saturation potential of −0.1 volt in time t4. For the case shown, measured t4 is 25 millimicroseconds (μsec) as observed with an oscilloscope having a total amplifier rise time of 10 μsec. Diodes D1 and D2 have been chosen to have minority carrier storage capability, for a given forward current, several times in excess of the storage capacity of the transistors due to excess injected minority carriers, for the same base current. Since D3, a storage diode as previously described, has a forward charge potential of approximately 0.7 volt due to carrier storage, the base of T2 will be driven rapidly toward a positive potential of approximately 0.6 volt by the collector of T2 going into saturation. During this period, part of the charge stored in D3 provides a recombination charge for the minority carriers stored in the base region of T2, thus reducing the storage time of T2 to a minimum. The illustration shown, the measured value of t4 is about 15 μsec. Minority carriers stored in diode D1 in excess of those lost in discharging the carriers stored in the transistor and those due to natural recombination are discharged rapidly via high-conductance germanium diode D6. Since the base of T2 is rapidly switched to the back-biased state, the collector fall time of T2 is also reduced to a minimum. (For the case shown, the measured value of t5 is 25 μsec.) The swing at the collector of T2 is limited by the forward conductance of D1 and the base-emitter junction of T2, thus terminating the transient condition of the transistors. The flip-flop circuit may be efficiently retriggered, this time by applying the current pulse to transistor T3 as soon as the excess carriers in D1 have been dissipated. Since the storage diodes have been selected to provide a minimum charge in excess of the worst case for carrier charge storage in the transistor for the same current, a designer must specify an upper limit for the minority carrier storage capabilities of a storage diode, as well as a lower limit if very high repetition rates are required. The Hughes type HD6172 storage diode, indicated in Fig. 4, will have sufficiently recovered within 2 μsec (microseconds), since the particular circuits under consideration had a maximum trigger frequency requirement of only 500 (kc) kilocycles. This specification includes diodes with a total charge storage for a forward current of 1 milliamper (ma) in the range of approximately 1 × 10−9 coulombs and provides a yield of about 90% when selected from the standard-type IN456 high-conductance silicon junction diode stock. The maximum charge storage due to minority carriers injected at an excess base current of 1 ma for the transistor used (type 2N383) is approximately 0.2 × 10−9 coulombs.

Fig. 6 shows the effect of the relative storage capability of two different cross-coupling diodes. In the case of the diode selected for lower storage, the diode sufficiently recovers in about 0.5 second discharging into the base clamp diode. In the case of the higher storage diode (total charge storage for a forward current of 1 ma being 3 × 10−9 coulombs) sufficient recovery occurs in approximately 1.5 seconds. By properly specifying diode and transistor storage characteristics, operation at trigger rates of 5 megacycles has been accomplished using type 2N393 transistors. Much higher rates are possible with a diffused base transistor (type 2N501) and with so-called "fast" silicon diodes to provide the desired cross-coupling characteristics.

In terms of circuit performance, the storage diode coupling technique provides several significant advantages over and above the rapid transient response obtainable through this technique. Excellent d-c stability results since the "on" transistor may be operated very hard in saturation and the "off" transistor is back-biased by an effective current source clamped by the base clamp diodes. Current mode operation is achieved in
switching the current in the collector load resistors between the saturated transistor and the cross-coupling diode. Since the desired cross-coupling turn-off charge is developed as a function of forward current in the cross-coupling diode, low collector voltage swings in the order of 1.5 volts are possible. If low input capacitance is desired in the conventional resistance capacitance (RC)-coupled flip-flop, the voltage swing is generally in the order of 4 volts, using similar transistors. The cross-coupling diode also provides very efficient base triggering of the flip-flop, since the base input impedance of the "off" transistor does not reflect the collector characteristics of the saturated transistor to any extent. This is due to the fact that the cross-coupling diode in the triggered output will be recovered or "open" in the reverse direction. The only shunting of the input pulse will be due to the diode capacitance which is in the order of $20 \times 10^{-12}$ farads.

**Current-Charge Mode Gating**

When considering a logical gating structure for a computing system, problems of compatibility between the gating and storage, or active, elements in the computer often arise. The gating structure within the system generally accepts the outputs of the storage elements, whether these be flip-flops, pulse amplifiers, or d-c amplifiers, and combines these, in accordance with the Boolean equations describing the system, to produce a logical output. This output then must be applied as the input of a storage or active element. When mechanizing a binary (2-state) logical structure, factors of importance in the gating techniques include:

1. Gating efficiency and the compatibility of the gates with storage and active element outputs.
2. Signal discrimination or the ability of the gates to detect the difference between a true and false proposition.
3. Compatibility of the gate output with the storage and active element input requirements.

When considering transistors for use in the storage and active elements, several facts are immediately evident concerning their input and output characteristics if they are to be operated as switches; i.e., in either a saturated or cut-off state with a required minimum transition time between these states:

1. To "turn on" a transistor in time $t_b$, the driving source must be capable of supplying a minimum current sufficient to charge the input capacitance and also to drive the transistor into current saturation.
2. Steady-state saturation requirements may be met by supplying a constant-current drive to the base.
3. The collector output characteristic of a grounded-emitter saturated stage provides an excellent constant voltage current sink.
4. To turn off a saturated transistor in time $t_1 + t_2$, sufficient charge must be drawn from the base to reduce rapidly the minority carriers during $t_1 + t_2$.

In the computer logical structure under consideration, a number of types of ac-
Fig. 12. Diode-transistor logic using storage diodes for fast turn-off

tive elements, or building blocks, are used. These building blocks differ in regard to their input requirements and output characteristics.

By employing high-storage silicon junction diodes in combination with fast diodes, a logical proposition may be gated in a manner compatible with the output characteristics and input requirements of the flip-flop previously described. Fig. 7 is the circuit diagram of a logical proposition mechanized in this manner.

As shown, the flip-flop trigger proposition is \( ABC(P_1) + DE(P_2) \). Terms \( (P_1) \) and \( (P_2) \) represent timing clock pulses which may be the main clock and occur every period, or may be the amplified result of still other logical propositions gated with the main clock and occurring only as these propositions become "true." In this application, the clock signal swings from zero to \(-2.5\) volts with a pulse width of 0.1 to 0.2 \( \mu \)sec. Propositions \( A, B, C, D, \) and \( E \) are normally developed by saturated or cutoff output amplifiers of flip-flops or d-c proposition amplifiers and inverters, as indicated. The proposition signal swings from saturation (approximately \(-0.1\) volt) to a clamped cutoff level chosen as \(-2.5\) volts. The saturated level is chosen as the zero or "false" proposition state while the cutoff level is the true state of the proposition. In this logical mechanism, "and" proposition diodes \( D_1, D_2, D_3, D_4, \) and \( D_5 \) are high-conductance germanium units chosen for their low forward voltage drop. Clock diodes \( D_6 \) and \( D_7 \) are high-conductance silicon units chosen for their minority carrier storage characteristics, as previously described. The "or" proposition diodes \( D_8 \) and \( D_9 \), as well as flip-flop input diode \( D_{10} \), are silicon units chosen for their forward conduction threshold and fast recovery characteristics.

It is noted that, with the exception of the clock diodes, the gate illustrated in Fig. 7 is a normal current mode gate with the current source supplied from B-minus through resistors \( R_1 \) and \( R_2 \). In the current mode gate, diodes \( D_6 \) and \( D_7 \) would be types similar to all proposition diodes. In the illustrated gating configuration, however, operation occurs in the following manner; first, consider only the upper "and" term of the "or" proposition when one or more propositions are in the saturated or false state. Under these circumstances, voltage \( E_i \) will be at a level of approximately...
applied, into the flip-flop using the combination current-charge gating technique (as considered in this application. One or more of the saturated proposition drivers will be supplying the necessary current to maintain this false or inhibiting level at $E_i$. Diode $D_4$ will be nonconductive since it is a silicon unit with a forward conducting threshold of about $-0.60$ volt. If a clock pulse ($P_l$) now is applied, $D_4$ merely reverse biases rapidly, since no minority carriers are stored in this diode. The only charge coupled to the "and" junction of the gate (i.e., at $E_l$) will be due to the small amount of capacitance in $D_4$. This charge is quickly absorbed by the propositions in the false state. This effect is shown for the inhibited case in the oscillograms of Fig. 8.

Assume now, that all propositions ($A$, $B$, and $C$) are in the true state. In this condition, clock diode $D_4$ will be conducting the total gate current (2 ma for this application) and a minority carrier charge will be stored in the diode. Voltage $E_i$ will be at about $-0.65$ volt, a level below the conduction thresholds of approximately $-1.35$ volts for the series input diodes connecting the "and" gate to the flip-flop unit. Upon application of the clock pulse $P_l$, voltage $E_i$ will rapidly be driven negative until the input conduction threshold is reached. At this time the clock diode will discharge into the input of the flip-flop, since the clock diode is back-biased. The second pulse in Fig. 8 indicates the result of a true proposition. The total charge $Q_t$, delivered into the flip-flop and associated stray capacitance is given by

$$Q_t = i_D \Delta t + Q_{st}$$

where:

- $i_D$ = the current in the gate resistor (considered constant)
- $\Delta t$ = the clock pulse width
- $Q_{st}$ = the charge transmitted by driving the clock diode in the reverse direction for a time $\Delta t$ with the peak inverse current limited only by the amplitude of the clock pulse and the series impedance of the circuit. The series impedance includes the clock pulse generator impedance, the instantaneous reverse resistance of the storage diode plus the impedance looking into the flip-flop.

In practice, the charge transmitted into the flip-flop using the combination current-charge gating technique (as compared to a straight current gate) is about three times greater at the signal levels under consideration in this application. Upon termination of the clock pulse, any charge left in this clock diode will be discharged by "false" going propositions. Fig. 9 shows the voltage wave forms at the "and" junction of three current-charge gates operating at 1 (me) megacycle as binary counter logic and using a 0.1- $\mu$ sec clock pulse.

Triggering a flip-flop using a combination current-charge gate offers a number of advantages over the straight current mode of operation. This is especially true when gating very narrow clock pulses using diode logic. For diode direct gate currents when using storage diodes, higher stray capacitance may be tolerated in the outputs of gates before malfunction occurs. Or, from another point of view, for a given input charge requirement, the gate direct current may be reduced, using the combination method. This enables a flip-flop output to drive more gates. Or, from still another point of view, flip-flop input trigger requirements may be made stiffer, thus reducing the susceptibility of the flip-flop to triggering on random transient noise. This is accomplished without reducing the number of gates which the flip-flop outputs may drive. The end result in each case is higher gatifying efficiency.

The added "booster charge" obtained by using this technique must be paid for, however. This additional charge must be supplied by the clock pulse driver. But the over-all power consumption of a computing system may still be considerably reduced, since clock power generally is made available at very high duty cycles, e.g., 10 to 1 or greater, when working at clock frequencies below 500 kc.

Current-Charge Gated Logical Clock Amplifiers

In large transistorized computers operating synchronously, total peak clock power requirements often are quite large. This demands either a vacuum-tube clock source, or multiple-transistorized clock amplifiers or repeaters enslaved to a master clock generator. The former often is undesirable because of the special requirements for power supplies, cooling, etc., not needed with transistor circuitry. Still another objection to supplying the total clock power, from one source is the problems encountered in transmitting very high-current pulses of very narrow width. The second approach is the commoner even though it is inefficient in terms of the total component count.

A more efficient technique, if over-all performance of a clock amplifier is considered as a measure of efficiency, is to provide clock repeaters in which the output pulse is controlled by logical propositions of flip-flops and d-c amplifiers, as well as providing clock amplifiers which repeat the master clock "one to one." These logical clock repeaters, generally amplifying clocked control propositions, then may be used to "and" with, and to clock flip-flop gates.

Fig. 10 is a diagram of such a logical clock repeater controlled by the proposition $(RST+XYZ)C_{pm}$. Here, $C_{pm}$ is the master timing clock. As with the previously described flip-flop gates, all proposition diodes are high-conductance germanium while the clock diodes, $D_4$ and $D_5$, are chosen for their minority carrier storage capability. In this case, unlike the flip-flop gate, "or" diodes $D_4$ and $D_5$, along with input diode $D_{11}$, are also silicon junction storage diodes. In the case of the flip-flop gate, these were fast silicon diodes chosen for their input threshold characteristic and ability to "disconnect" rapidly upon termination of the gated clock pulse. Fast disconnect is not desired in the input to logical clock amplifiers.

The action in "turning on" the logical pulse amplifier of Fig. 10 is identical to the action described for the flip-flop gate. During this clock pulse duration, however, diode $D_4$ or $D_5$ and diode $D_{11}$ store minority carriers several times in excess of the carriers stored in the transistor base region. Upon termination of the gated clock pulse, therefore, the voltage $E_a - E_b$ (for the case where proposition $RST$ is active) is about $-1.3$ volt, where $E_b$ is equal to the base-emitter drop in the "on" transistor. Diodes $D_4$ and $D_{11}$ are effectively charged to a potential of about 1.4 volts, a value dependent upon the instantaneous reverse characteristics of the diodes when subjected to the forward current during the clock width, $\Delta t$. Since the charge storage capabilities of these diodes greatly exceed that of the transistor used, $E_b$ will be driven rapidly to a potential of about $+0.6$ volt during the positive transition of the clock pulse, rapidly discharging the carriers stored in the transistor and reducing its storage time ($t_s$) and fall time ($t_f$) to a minimum.

Fig. 11 shows oscilloscope wave forms at points of interest in this circuit in which 0.1- $\mu$ sec pulses are being logically gated. In the circuit shown, the output current pulse is in the order of 150 ma at 2.5 volts.

Diode-Transistor Logic Using Storage Diodes for Rapid Turn-Off

Still another useful application for storage diodes is in connection with...
diode-transistor logic. Fig. 12 shows a typical gating arrangement in which "and" propositions are possible and generally are a requirement in computers. The clocked "and" proposition is used for triggering a flip-flop or logical clock amplifier. The trigger clock in the case of flip-flop logic may be any logical clock or repeated main clock. One clock, however, multiplies each "or" term of the flip-flop input. Fig. 14 illustrates a typical combination. "And" propositions gating the inputs to logical pulse amplifiers are always referenced back to the master timing source, $C_{pm}$. This prevents the accumulation of delays or the staggering of clock pulses which trigger flip-flops. The second type, or unclocked "and" proposition, is used for driving d-c amplifiers which may be combined as illustrated.

The techniques described have been applied to computers having both serial and parallel arithmetic structures. The complexity of the logic and clock repetition rate determine to a great extent the arrangement of the various building blocks. For example, in the case of a 20-bit parallel arithmetic unit, the propagation of the "carry" for the binary accumulator is readily accomplished at a 200-kc clock rate using the diode-transistor logic described. Here, assuming the worst case where the delay is 0.15 $\mu$sec per carry stage, all d-c amplifiers will have settled down in 3 $\mu$sec, thus allowing ample safety factor in clocking the accumulator register to produce an addition in 5 $\mu$sec. Using the storage-diode flip-flop trigger technique, it is noted that a few tenths of a microsecond are required to discharge the clock diode into the proposition for the case of the proposition going false before clock time. Also, for the clock storage diode to be effective, a proposition must go true a few tenths of a microsecond before clock time so that the gate current may be integrated to provide sufficient carrier injection in the diode. For performing this current integration, the storage diode, unlike a capacitor, is extremely nonlinear in that it becomes saturated in the forward direction in a few tenths of a microsecond, operating at the gate current of 2 ma.

Conclusions

In this paper, techniques have been described which utilize the inherent minority carrier storage effect exhibited by high-conductance silicon junction diodes to improve transient response in digital switching circuits. Attempt is made to combine both slow and fast diodes with transistors in a manner which most effectively complements the fundamental characteristics of each semiconductor.

References

Discussion

Chairman Ruhman: The first question for Dr. Poppelbaum is from A. I. Gordon, Hughes Aircraft Corporation: “What would the necessary voltage swing be for a Schmitt-trigger?”

W. J. Poppelbaum: About 20 volts.

Chairman Ruhman: From J. H. Lane, ElectroData: “Just why do the transistors require such relatively high betas?”

W. J. Poppelbaum: The high beta is required so that you do not have too much loading between supply and the ground. It just limits you in the low rate because you have too much reflective on the base side.

I should point out, incidently, that these flip-flops at the University of Illinois are first open to mated, a certain relations method. Then you will find out that under the worse cores and conditions the thing still works.

Chairman Ruhman: from Mr. Klein, Magnavox: “You explained how the signal flow is gated; would you mind explaining how the desired drivers are selected? What kind of gating do you use for them?”

W. J. Poppelbaum: You use the output.

Chairman Ruhman: From H. Tweeden, General Electric Company: “What is the over-all delay of this circuit?”

W. J. Poppelbaum: The over-all delay is 15 micromiloseconds. This is ficticious, of course, as it takes time for this kind of a swing.

Chairman Ruhman: From F. W. Springe, Hughes Aircraft Corporation: “What are the space (packaging) considerations of low gating compared to gating with the regular Eccles Jordan?”

W. J. Poppelbaum: I should actually say that this system was developed to provide very small buffer registers. We do have plug-in units. There were 15. One half unit by a quarter by a quarter.

Chairman Ruhman: From P. Writer, Litton Industries, Inc.: “What methods are used to connect leads to the modules? If you use connectors, what kind?”

Arney Landy, Jr.: We have used the flexible lead, just as in a transistor placed in the circuit board. With regard to connectors of the body to circuit, there is work going on at Honeywell regarding soldered connections. I can see by Mr. Writer’s questions, that he too is concerned by the connections, number of them, and number of components and also getting a good connection.

Chairman Ruhman: From A. I. Gordon, Hughes Aircraft Corporation: “What is the dissipation derating factor for compound used? How are resistors derated? Does this element meet Mil-specifications?”

Arney Landy, Jr.: I believe your first question refers to billing compound or plotting. We intend to use the 10 wad or 8 wad.

Does the element meet the Mil-specifications? I am not sure, but I see no reason why it will not.

Chairman Ruhman: From Mr. Dunnet comes from Mr. Fink, Hughes Aircraft Corporation: “What type of cores have you been using in this circuit?”

W. J. Dunnet: One-megacycle design that we built in the laboratory. We used 18,473 crips without much iron.

Chairman Ruhman: From V. W. Vordran, Hughes Aircraft Corporation: “What type of core is used? What are number of turns? What are control and clock current amplitudes?”

W. J. Dunnet: I could use almost any number there. As a matter of fact, we have. The most might have 20 turns. About 10 on the input windings. We are planning to use something like 500 mils to reset the cores.

Chairman Ruhman: From W. E. Ross, Litton Industries Inc.: “Why not take advantage of regeneration by using a collector winding?”

W. J. Dunnet: I do not know if I can answer that question. You do not get much by regeneration of reverse write where they use regeneration. It might cause more problems, or we might gain by it. I do not know. Actually, we have not been too concerned with it. I would like to think about it for a while before I even consider it.

Chairman Ruhman: I would like to ask a question myself. “Could you, very briefly, indicate what you think the advantages are of this circuit over some of the other types of magnetic circuits as have been used for logic?”

W. J. Dunnet: The advantages would be the advantages I showed on the board. The simplicity of the thing.

Perhaps, in 6 months or a year we will be able to say more as to just what the advantages are, after we have actually built one.
A Chess Playing Program for the IBM 704

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This paper describes the program which enables a human being to play a game of chess with the International Business Machines Corporation (IBM) 704 computer. The machine may play either white or black, and is capable of playing a complete game of chess, including such moves as casting, promoting, and capturing en passant.

The program is divided into five parts: (1) Input-output, (2) Table generation, (3) Evaluation, (4) Decision, and (5) Tree.

Input-Output

The input-output section of the program allows the human player to state his moves to the machine in the normal English notation on punched cards, for example: P-K4 or B(Q4) x P(N7). The program then translates this statement into the machine notation for moves, which gives the "to" square and the "from" square with a code. A move in the machine notation may also be entered from the keys on the console.

The squares of the board are numbered octally from 00 in the upper right-hand corner of the board to 77 in the lower left. For a regular move, the tag field contains a 1, the decrement contains the "from square" co-ordinates, the address contains the "to square" co-ordinates, and the prefix contains a minus sign if the move is a capture. For a castling move, the tag field contains a 2, the decrements contain the "to square" of the king, the address contains 77 if castling up, 0 if castling down, and the prefix is 0. (Castling upwards means that the final position square of the king has a higher number than its initial square.) For an en passant capture, the tag field is 3, the decrement contains the "from square" of the capturing pawn, the address contains the "to square" of the capturing pawn, and the prefix contains a minus sign. For a promotion, the tag field contains a 4, the decrement contains the "from square" of the pawn that promotes, the address contains the "to square" on which promotion occurs, and the prefix contains a minus sign if the move is a capture.

At the start of a game the machine’s pieces always reside on the squares 00 to 07, 10 to 17; the opponent’s on the squares 60 to 67, 70 to 77.

If the machine were to play white and make P-K4 as its first move, in machine notation this would be the octal word, 000114100034.

When the machine has made a move, or accepted an opponent’s move, it prints that move in the English notation, together with a picture of the board position, and makes a record of the move on tape. At the end of the game the full score is printed.

Table Generation

The table generating section accepts as its input a table of the board position which will be referred to as TA1. TA1 at the beginning of the game is arranged so that it represents the starting position; but any board position may be assembled into TA1 and entered as the starting position for the program.

TA1 is 64 words long, one word per square. The first word of TA1 refers to square 77, the last word to square 00. If the square is empty then the word is all zero. The word is negative if the square is occupied by a machine piece. The address contains a number indicating whether the piece is a king (5), queen (0), rook (1), knight (4), bishop (2), or pawn (3), and the decrement contains an indexing quantity to link TA1 with Table 2, which will be called T42.

T42 is now generated from TA1 in the following form. It is 32 words long, one per piece. The order is shown in Table 1.

A word in T42 is of the following kind: It is zero if the piece has been captured. Otherwise, the address contains the value of the piece, and the decrement contains the co-ordinate of the square where the piece is located. It can be seen that the decrement of T42 is the indexing quantity of TA1.

Table 31 and Table 32, called TA31 and TA32, are also generated from TA1. TA31 refers to the machine and TA32 to the opponent. TA31 and TA32 are similar in nature and function. Thus it is sufficient to describe TA31.

TA31 is 512-words long, eight words per square. The first eight words refer to square 77 and the last eight words refer to square 00. Consider the eight words referring to square (xy). If the square xy is occupied, the eighth word is negative, and contains a hit in the first position if it is occupied by the machine but not if occupied by the opponent. The address of the eighth word contains:

1. The number of machine pieces which may move into square xy if xy is empty.
2. The number of machine pieces which may immediately capture an opponent’s piece situated on xy.
3. The number of machine pieces immediately defending a machine piece situated on xy.

The location of the pieces described in the address of the eighth word are in the decrements of the words 8 through 1. The address of the seventh word stands for the number of doubled machine pieces bearing on square xy, e.g. a rook behind a rook bearing on xy, or a queen behind a bishop, etc. The location of these doubled pieces are to be found in the addresses of the words 6 through 1.

It will be seen that the location of the pieces bearing on xy is the indexing quantity needed to find that piece in TA1, while each square xy in TA3 is eight times the indexing quantity of TA1.

All possible moves are now listed in TA3, for each square has in it the number and locations of all pieces which may move into it.

The routine which generates TA3 also examines the position for any possible pieces pinned to the king, so that no illegal moves are listed in TA3.

TA2 and TA3 are generated in an average time of 89 milliseconds.

Evaluation

The evaluation routines calculate a score for the machine and the opponent based upon the following criteria:

1. Mobility
2. Area control
3. King defense
4. Material

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