The RCA 501
Electronic Data Processing System

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The RCA (Radio Corporation of America), 501 Electronic Data Processing System is a complete and new system in the intermediate- and large-scale performance class. It is a general-purpose system using all transistor logic. The system has been under development for approximately 3 years. The efforts of this program have resulted in a prototype system which is presently in test.

This system is distinguished by the following features:
1. High rates of data transfer are provided by magnetic tape, with complete retention of accuracy control measures.
2. The units comprising the system are completely transistorized.
3. The system is easily expanded in terms of high-speed memory capacity, number of tape stations handled, large scale random access memory, and input-output capacity.
4. Completely variable data organization is enhanced in the RCA 501 system.
5. Simultaneous compute functions with magnetic tape, printer, and paper tape reader operation are provided.
6. Programming flexibility is keyed to maximizing equipment usage with ease.
7. New versatility is provided for magnetic tape handling and address modification.

The system design for accuracy control is based upon a proper balancing of component reliability and built-in measures for checking data transfer and manipulation.

The RCA 501 Electronic Data Processing System is comprised of a computer and both on and off-line input-output units.

The RCA 501 computer actually consists of a number of integrated units. It includes a console, program control, high-speed memory, monitor printer with paper tape punch, paper tape reader, and associated power supplies.

The console typifies the functional design and human engineering which was applied to all units of the system. The console provides for complete monitoring of computer operation, including display of pertinent register and status level action during program testing and maintenance periods.

The program control facilitates addition of up to 63 tape stations, up to 262,144 characters of high-speed memory, and on-line high speed printing. It is basically a modified two address system for use with completely variable data organization.

Program control provides for electronic switching of up to eight tape stations. Additional increments of eight tape stations are provided by tape selecting units which connect to the basic tape selecting unit of the program control. Maximum capacity of the program control is 63 tape stations. Switching time is negligible at the approximate level of 10 microseconds.

The monitor printer is mounted on a separate table and includes a paper tape punch. Its basic use is for operational control, program testing, and exceptional types of output.

The paper tape reader is under program control and operates at the basic rate of 400 characters per second. The paper tape reader with its reel mountings is housed in a separate cabinet.

The computer high-speed memory is available in increments of 16,384 characters up to a maximum of 262,144 characters. All character locations are individually addressable. In one 15-microsecond cycle, the programmer has access to any one character, or four characters in parallel, with regeneration included. (See Fig. 1)

The RCA 501 tape station has a read-write rate of 33.3 kc and moves tape 100 inches per second either forward or reverse. (See Fig. 2)

Input equipment in the RCA 501 is designed to accommodate expansion. Eighty column cards are converted to magnetic tape in two ways. A card reader transcribes directly to magnetic tape with editing reserved for the computer. This same unit may also be connected to a card editor which edits each card and records these data on tape in accordance with a programmer-prescribed message format. The combined unit is referred to as a card transcriber. The card reader transcribes cards at a maximum rate of 400 cards per minute. Fig. 3 illustrates one view of the card reader.

An RCA 501 tapewriter and tape-reader-verifier are included in the product line to handle the original preparation and verification of punched paper tape for subsequent on-line transcription into the system using the paper tape reader.

The output equipment is similarly designed to permit convenient expansion. A line printer is provided in the system which is designed to operate on-line from the computer or to operate off-line with a data editor. The on-line printer accepts edited data and is controlled by the computer. The off-line electro mechanical printer is formed by driving the line printer from the data editor. Editing control is provided by a plugboard and a tape loop for complete horizontal and vertical editing of data received from a magnetic tape. Fig. 4 is a view of the printer mechanism which prints at the rate of 600 lines per minute and up to a 120-column line.

In order to accommodate the punching of 80 column cards from magnetic tape, a transcribing card punch is included in the system. This unit provides for punching of cards at a maximum rate of 100 cards per minute.

Large scale random access memory is also available for on-line operation with the RCA 501 computer. A random access file control unit which provides for connection of up to 32 random access files is provided for direct trunk connection to the computer. Each random access file will store 1,500,000 characters with the average random access time to any data being 192 milliseconds.

The RCA 501 tape station handles magnetic tape which is 3/4 inch wide and available in 2,400-foot reels. The recording density is 333 1/3 characters per inch and tape speed is 100 inches per second in forward or reverse. Dual recording of data is retained as a primary accuracy control measure and also to enhance magnetic tape life. Each information bit is recorded on two separate tracks on magnetic tape, each one of which is capable of producing a standard signal during reading.

Transistorization

Probably the most significant engineering advance in the RCA 501 Electronic Data Processing System is the completely new all-transistor logic. Working in conjunction with the RCA laboratories in Princeton, N. J. the Semiconductor Division, was able to specify...
and tests types of transistors uniquely suited for the system application.

Transistor types resulting from this work are now being used in the RCA 501 system circuits and logic packages. The use of transistors has increased reliability, reduced physical size, and reduced power requirements.

For a computer with a high-speed memory capacity of 32,768 characters, approximately 14,000 transistors are used. The transistors are mounted and dipped soldered on small printed wiring boards, as seen in Fig. 5, which in turn are dipped soldered to the larger printed wiring board.

Over 90% of the system is constructed from one basic normal operation register, (NOR) circuit, which is wired on the small boards referred to as a submodule. This circuit is a two-input-type unit used for AND, OR, power and indicator driver circuits. It is also used to construct flip-flop register circuits by cross coupling the inputs and outputs. The printed wiring pattern on the large board dictates the plug-in logic configuration. Plug-ins are assembled in a rack as shown in Fig. 6.

**Expansibility in the RCA 501 System**

Expansion is built into the RCA 501 system in terms of the number of tape stations and tape selecting units used, in the capacity of high-speed memory, and in the type of input and output units.

These features are provided by a system design which minimizes user investment during initial stages of program testing, conversion, and production. Further, these provisions are made to permit the user to expand his production in terms of volumes and variety of operations. All of the features are designed in such a way that major disruption of the operating installation is avoided.

The basic tape selecting and buffer unit in program control, permits connection of one to eight tape stations to the computer. (See Fig. 7). For the purpose of expansion, each trunk line so provided may be connected to a tape selecting unit-B which has eight additional trunks, each of which can be connected to tape stations or file control units. With the addition of these units, the system can be expanded to include up to 63 trunk lines to the computer. (See Fig. 8).

The expansion of the system in terms of total number of tape stations connected to the computer and the increase of the high-speed memory from the basic 16,384 characters in modules of 16,384 characters to a total of 262,144 characters are both directly related to the scope of the application handled, as well as the over-all efficiency of the system. Tape station and high-speed memory increases add measurably to the efficiency of sorting and merging. They add substantially to the procedural content of computer capabilities in terms of greater program capacity and the introduction of a wider variety of input and output types to each operation.

Input and output volumes are related directly to the need for expansion from on-line forms of input and output to off-line forms. In addition, the introduction of the card editor and the data editor as parts of the card transcriber and electromechanical printer respectively, improve over-all system efficiency by providing parallel operation and greatly relieving the computer of editing chores.

**Data Organization**

Completely variable data organization is enhanced in the RCA 501 system. The processing of data in its most natural form, avoiding arbitrary restrictions and editing procedures, is the design objective. Binary coded RCA characters consist of six information bits and one parity bit. The RCA code is alpha-numeric, including all letters, numbers, punctuation and special marks, and control symbols. In the RCA system, characters necessary to specify a particular unit of information, such as a stock number or a policyholder's name, are organized as items in their natural form. These items are organized into messages which have unique significance, such as policyholder's reference file, a transaction, etc. A second form of data may be written on magnetic tape without regard to message structure. These data are referred to as a block and consist of eight or more characters which may be handled by the computer for special applications.

The natural computer language, namely the handling of data in the form in which it occurs or in the form in which it corresponds to procedural logic, is a system advantage which increases the efficiency of all equipment items in the system and in particular the effective utilization of tape stations, high-speed memory, and the computer proper. Actual experimental analysis of applications converted to RCA electronic data processing systems reveals a far greater return in terms of data storage reduction than was originally anticipated.

**Computer Logic and Simultaneity**

The computer logic design uses a two address instruction code which is made
up of eight characters. One character specifies the operation, three characters each specify the two addresses A and B and one character specifies the N code. The N code is used to call for either one or two out of seven static or dynamic register locations. Static registers refer to high-speed memory storage locations, whereas dynamic registers refer to flip-flop-type registers since the contents may constantly change during the operation cycle of an instruction. The contents of these registers are added to either or both of the addresses A and B. The instruction is then executed by using the sum of the address(es) and the modifier as the final address(es). This modification does not alter the instruction stored in the high-speed memory.

The execution time of an instruction depends upon the instruction and the data being processed. For example, in a decimal addition, the instruction performs an end-around carry or is terminated after processing the most significant digits of the operands and the operands’ length may be completely variable.

The instruction execution time is the sum of a series of 15-microsecond status levels, each of which is equal to the memory access time. The status level is in turn divided into series of six time pulses each 2.5 microseconds in duration.

The computer uses a bus scheme as shown in Fig. 9. All registers have access to those buses, thus permitting the programmer a high degree of freedom in transferring and storing data and address information in the registers. Registers are used in place of address counters. A simplified binary adder is used to modify the contents of registers on the memory addressing bus by addition or subtraction. This permits character location addressing in either an ascending or descending mode, which in turn adds versatility to data manipulation.

As seen from the Fig. 9, simultaneous access to four characters is possible. This decreases the time required for forming and data transfers. No data-length restrictions result from this arrangement, since all character locations are individually addressable.

Simultaneity in the computer has been added to make use of the low access cycle of the high-speed memory during the execution of certain instructions. For example, most of the execution time of a tape instruction is consumed in tape movement. Therefore, an interrupt technique is used which permits a compute function to proceed simultaneously with a second instruction. The compute instruction is interrupted only when access to the high-speed memory is required by data as controlled by the second instruction.

To accomplish this, a normal (NOR) and a simultaneous operation register (SOR) is used as shown in the diagram. These registers specify the operation in process, such as decimal add, etc. Instructions are performed in either the normal or the simultaneous mode. All instructions are initiated and may be performed in the normal mode, but only potentially simultaneous operations may be performed in the simultaneous mode. Potentially simultaneous instructions include certain magnetic and paper tape, monitor print, on-line printer and random access File operations. If the simultaneous mode is free, transfer from the normal to the simultaneous mode will take place by transferring the contents of NOR to SOR and A register to S register. This transfer is normally automatic but may be controlled by the program. If the simultaneous mode is already in use, the transfer of the potentially simultaneous instruction from normal mode will take place upon completion of the simultaneous instruction without interruption and regardless of how far the instruction has progressed in the normal mode. Upon completion of this transfer the next instruction is formed in the normal mode and the execution of it initiated.

Another technique of value both functionally and economically is incorporated in the on-line printer logic. The on-line printer consists of a rotating, etched character drum with an attached character identification and timing disk. Solenoid driven hammers strike the paper, forcing the paper and a carbon ribbon against the rotating drum for character printing. Paper motion equipment is also included. Each one of the 51 print characters, such as the "A," is etched in line for a total of 120 positions and the whole line is parallel to the drum axis. Thus, all similar characters in one print line, such as the "A," are simultaneously printed. A line of print is complete after one complete drum revolution. The logic to perform this function requires that the printed data be edited in the computer. These data from the computer are compared against the character identification disk, the results of which
Fig. 7. The basic RCA 501 system

are transferred into a 120-position shift register. The characters of this drum line are printed by parallel shifting this information out of the shift register. This information in turn drives the print hammer solenoids. Following this, the next character compare cycle begins. The process is repeated for each print character until a complete line is printed. The computer then instructs the printer to advance the paper through the desired number of lines.

Programming

Programming complexities are normally traceable to the difficulties imposed by the inherent design of a data processing system when attempting to realize the full potential of the system’s effective capacity.

One important programming feature of the RCA 501 computer is the provision for automatic relative addressing of both programs and data. This feature is facilitated by the availability of the static and dynamic registers which are under programmer control. Beginning and end addresses of variable size messages are located by use of static registers. Within a message, any item may be located by use of the “locate nth symbol” instruction. Relative references can be made to a series of consecutive items by using final contents of the registers, which are dynamic registers. When processing reference files using the simultaneous tape instructions, it may be desirable to have alternating areas for reading and writing.

The ability to alternate data areas in this fashion evolves in the 501 computer the simple problem of transposing the contents of two of the static registers. In this way, extensive program modification or duplication is entirely avoided.

Fig. 8. An expanded RCA 501 system

Fig. 9. The RCA 501 computer, block diagram

Programs can be written relative to a fixed point by utilizing static modifier registers. In order to float or transfer addressing of programs, it is necessary only to relocate the program in the memory and change the setting of the register. Programs can also be written completely self-relative for the computer. The programmed instructions are set up so that they are relative to the setting of the program register, the contents of which hold the high-speed memory location of the next instruction to be executed. This is the P register shown in Fig. 9. Programs written in this manner can operate without modification from any position in the memory.

Another over-all feature of the RCA 501 computer is the emphasis upon efficiency in tape handling. Sorting is improved substantially by the incorporation of reverse read, the use of locate nth symbol, four-character parallel transfer, modifier register operation, and by programmer access to all registers. Batching of messages after internal block sorts is itself facilitated by locate nth symbol, multiblock write, and directly addressable tapes.

The handling of transaction input and reference files is greatly improved by binary operations for sensing, random distribute and multiblock write for data handling, and the miscellaneous features for data shuffling such as are provided by reason of an individually addressable character memory and control symbol logic as provided by the RCA 501 computer.

Accuracy Control

Extensive field experience with other RCA computing systems has permitted the adoption of a well-balanced approach to accuracy control in the RCA 501 system. Both equipment and programmed checks are used. Evaluation of the system logic, coupled with field experience pinpointed critical areas where hardware checks were required. Areas

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of a less critical nature may be program
checked, thus avoiding unnecessary check-
ing circuitry. But, in all cases, the in-
formation is checked in each unit as it
flows from the system input to the system
output.

Several types of equipment checks are
performed in the system. Included in
these types of checks are parity, all and
only, double arithmetic and compare, tape
data format, dual recording, and echo
checking.

A seventh bit is added to the six-bit
character which provides a parity count
to insure against the loss of bits. In
general, parity is checked whenever
data enters or leaves a unit in the system.
In the computer, parity checks are per-
formed whenever data are internally
transferred.

The all and only checking feature in-
sures that all and only those characters
to be processed are actually processed.
These checks are found in equipments
such as the electromechanical printer and
the card transcriber.

The double arithmetic and compare is
used in the computer to insure correct
operation of the adder. This check in-
volves the comparison of the arithmetic
result against the complemented arith-
metic result which also includes the com-
plemented carry. This check is per-
formed on a character by character basis,
thus permitting variable length operands
and result, without restriction.

The tape data format check insures the
proper organization of data on tape by
checking the sequence of special symbols
as the information is written on, or re-
ceived from tape.

Dual recording of magnetic tape in-
formation is used to insure reliable read-
and enhance tape life. Two tracks
representing each bit are displaced by
approximately half the tape width and
are serially connected, thus writing iden-
tical information in two tracks of the tape.
Information read from either track of
the tape is sufficient to provide the cor-
rect output.

The echo check feature verifies the
parity of the tape-head writing current
to insure correct receipt of data at the
tape head.

Summary

In summary, the RCA Electronic Data
Processing System is presently under-
going prototype tests in Camden, N. J.
First production systems will be delivered
in the last quarter of 1959.

This system is intended to provide for
closer fitting of an equipment system
to application characteristics. The sys-
tem design provides for this fit at mini-
num user investment levels. It also
provides for graduated levels up to a
maximum efficiency level which is geared
to fit large scale application requirements.

The major engineering advance of all
transistor logic is directly related to
an objective for substantially improving
the reliability level of a data processing
system with corresponding reductions
in power, size, and over-all system
cost.

The Univac® M-460 Computer

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THE Univac M-460 is a computer of
advanced design from both the logical
and engineering standpoints. It is the
intent of this paper to describe its more
interesting features.

The Univac M-460 computer is a large
scale high-speed general-purpose digital
computer especially suited to rapid, com-
plex processing of large quantities of
data. The computer is a parallel, single
address computer with fixed point,
one's complement binary arithmetic.
A computer word in the M-460 is 30 binary
digits in length with the provision for
treating the two 15-bit halves independ-
ently, if desired. The memory section
has a capacity of 32,768 30-bit words with
a cycle time of 8 microseconds, and a read
access time of 2.5 microseconds.

Special advanced logical features give
the M-460 a great deal of programming
flexibility. From the standpoint of the
number of instructions required for a
given operation, the effect is much as if
two-address logic were employed.

For purposes of discussion, the com-
puter may be divided into four sections:
control, arithmetic, input-output, and
memory. The block diagram of Fig. 1
shows the interconnections of each of the
four sections. The main registers of the
computer are shown by rectangles.
Some of the principal functions of each
section are indicated within the round-
edged blocks.

The control section includes a 30-bit
instruction register U, a 15-bit program
address register P, seven 15-bit address
modification registers, B1 through B7, and
a 15-bit auxiliary register R. A computer
instruction is executed by first acquiring
an instruction word from the memory
location designated by the P register and
then performing a number of operation
sequences controlled by the instruction
register U. Normally the content of the
P register is advanced by one count for
each instruction so that instructions are
executed in numerical sequence. Pro-
gram branching may be performed by
changing the contents of the P register in
jump instructions. A special feature of
the control section permits program
branching by another method. A skip
designator, active in most instructions,
permits an extra one-count advance of

the P register if certain arithmetic
criteria specified in the instructions are
met. Thus the next sequential instruc-
tion may be conditionally skipped.

The organization of the instruction word

Fig. 1. Block diagram showing the inter-
connections of the four sections

Fig. 2. Organization of the instruction word