1. The digit counter which counts the number of characters in a word (optional 5, 6, 10, or 12).
2. The data group counter (optional any number from 1 to 10).
3. The sample counter (optional 1, 10, 15, 20, 30, 45, 60).
4. The block gap generator (optional, any time).
5. The parity check generator (optional odd or even check) and several more.

The selection of a specific performance is done by two means, patchboard and switch.

**Patchboard**

A 100-point patchboard allows the selection of all formats in Fig. 7 and additional specific modifications. Normally, one format is needed corresponding to the local computer. However, in some places there are different computers available, for instance, a smaller local computer for quick evaluation and a big central computer for final evaluation. Sometimes two different central computers are available and the selection depends upon their work load, so, a fast format change is then needed. Some tests may be made twice in two different formats in order to make greatest use of the computer facilities. Then, the number of wanted formats is patched and specific points patched to the switch inputs.

**Format Switch**

This is a multiple, double-throw switch, which effects a fast change of the patching pattern. Two or more different formats may, thereby, be selected by the turn of a knob.

Standard selections could be:
- IBM 704, sb (format 1)
- IBM peripheral, bcd (format 6)
- IBM 704, and peripheral (format 4)
- Remington Rand 1103, sb. (format 13)
- IBM 650 (format 12)
- MilliSADIC card punch (format 8)
- or any other combination

It should be kept in mind that the data processing speed is different for the different formats. This may motivate the computer and format selection. It also shows the influence of the "contrasts in computers" on the data-acquisition systems and thereby on the original test itself. It is believed that the Micro-SADIC system succeeds in giving the liberty to scientists and engineers to select the best way for their data processing problem. However, the limitations inherent in the computer characteristics can not be avoided.

**The Over-All System**

The beginning of this paper mentioned the importance of high speed in data processing, high accuracy, reliability, flexibility, and completeness as main system characteristics. The following figures show how Micro-SADIC is able to realize the following goals:

**Maximum Speed**: Format 16: 10,000 samples per second average, s.b. code, each corresponding to 3 decimal digits. (20-ke clock rate)

**Accuracy**: ±0.1%

**Reliability**

Industrial reliability can be defined as the ratio of working time to trouble-shooting time for the system. The working time is mostly given by the components' life time. Micro-SADIC uses only long life components and transistors as active elements. The circuit design tolerances correspond to the known end-of-life values for each components for instance ±15% for resistors. The trouble shooting time is greatly reduced by Micro-SADIC's modular and operational design and numerous checking and test facilities, marginal checks included.

**Flexibility**

The writing of 16 different formats is standard. Additional modifications are possible. Two different codes can be written. Input data can be digital, analog, or pdm.

**Completeness**

Special equipment (specific transducers, code transformers, etc.) allows system combinations for practically all tests. The standard equipment covers the essential applications as known from the past and expected in the future.

**Experience**

In order to give an idea of the background of the data acquisition technique, it can be stated that 30 data-preparation systems (SADIC and MilliSADIC) have been installed during the last 5 years by this company only. Micro-SADIC represents the latest state of the art in components, manufacturing, and systems design.

The MicroSADIC provides an efficient input means to many computers with their contrasting input conditions.

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**A Computer-Integrated Rapid-Access Magnetic Tape System with Fixed Address**

**R. L. Best**  **T. C. Stockebrand**  **Nonmember AIEE**

This paper describes the internal tape library system planned for the TX-2 computer at Lincoln Laboratory, Massachusetts Institute of Technology (MIT). One hundred magnetic tape transports will be under the control of a central electronic system; the system will have a storage capacity of 10^6 bits and an access time of about 30 seconds. It is particularly well suited for use with a computer of large random-access storage capacity such as TX-2, which has a core memory of 21/2 million bits. A simple tape transport having a high-speed search mode with redundant information transfer will make the ultimate library system for a computer, reliable and relatively inexpensive.

The tape transports are controlled by electronic circuits closely integrated with the computer. A permanent, constant-density timing track on the tape provides the speed reference for the control circuits and makes possible fixed position address-

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put stages are normally saturated and the gain need not be closely controlled.

Computer/Tape Library Relationship

The primary objective, a large library of quickly accessible information, is provided by a large number of tape transport mechanisms controlled by a small number of circuits which are closely integrated with the computer. One feature of TX-2 is its multiple sequence control; that is, it can share its attention between equipments which are operating simultaneously in real time. The computer commands the selected tape drive to attain some mode of operation, then turns its attention elsewhere until the tape control tells the computer that the desired mode has been attained. Multiple sequence control also enables the computer to vary the speed of the tape during information transfer: this feature would be used, for example, if the computation itself depended upon external, real-time events and the information transfer had to be synchronized with the results of the computation.

Another feature of TX-2 is its large, random-access core memory which can store large blocks of information at one time and which can be used as a buffer while the tape is accelerating. The control element for the tape library accepts the computer’s commands rapidly but does not require instant response by the computer to events in the tape system. Generally the control takes care of the simple local problems and leaves the complex problems of operation to the computer, and therefore the programmer.

The tape mechanism, which has a wide variety of speeds, can search through a reel of tape much faster than the computer can accept information. For this reason, blocks of information on the tape are tagged with block marks that can be read at speeds up to the maximum, 920 ips. The read and write instructions command only a single 9-bit transfer between memory and tape. A series of such instructions is necessary to transfer large blocks of information; the instructions must occur at an average rate determined by the tape’s speed.

Transport Design and Motion Control

Mechanical Design

The tape transports used in this system were made as simple and fool-proof as possible: they consist of a read-write head assembly, two reels, two drive motors, and a tape guide. The drive mechanism has no capstan. Thus a good deal of mechanical complexity is eliminated and a wide range of tape speeds is made possible. Fast starts and stops are precluded, however: 1/2 second and 7 1/2 inches of tape are required to reach 30 ips.

Figs. 1 and 2 show the transport mechanism. The motors are flange mounted, 1,800 rpm, 3-phase induction motors of the conventional type which have roughly constant torque characteristics when operating well below synchronous speed. The horsepower (hp) rating, and therefore the torque, is as high as possible, limited by the tensile strength of the tape. One-eighth-hp motors, each driven by a magnetic amplifier, provide the proper torque to operate 10-inch reels mounted directly on the motor shaft and loaded with polyester tape, 0.001-inch thick and 1/2-inch wide. Maximum tape speed is about 920 ips when the driving reel is full.

The head assembly and guide are shown in the insert, Fig. 2. The relatively large, constant radius of the guide reduces the pressure between tape and guide: At speeds above 20 ips the tape floats on an air cushion and is thus easy to edge guide. Skew, caused by non-uniform tape tension across the width of the tape and by variations in tape width
is minimized. There is no wrap around
the head. Variations in tape tension,
which are large in this transport, do not,
therefore, cause excessive pressures on
the head and wear is reduced. Because
only short wave lengths (0.0025 and 0.005
inch) are used in the system, the area of
tape-head contact need not be large.

The direction in which the transport
is moving is determined by a sensing
device mounted on the rear shaft ex-
tension of one motor. The sensor con-
ists of an iron cup dragged against one
of a pair of stops by hysteresis from a
star-shaped permanent magnet on the
motor shaft. The cup operates a mercury
switch by rotating an attached magnet.
This scheme gives positive direction
information even at the slowest tape
speed. A mercury wetted contact switch
provides computer-level signals to the
control without contact bounce and with
good reliability.

**Motion Control**

Each motor can generate torque in only
one direction to pull the tape from one
reel to the other. The control of the
motors is therefore simpler than if torque
had to be reversed. Since tension is
limited by tape strength, acceleration is
relatively slow. A sudden change of
torque, which might allow a loop to form,
is prevented by a long time constant in
the control windings of the motor mag-
netic amplifier.

To stop the tape, full torque is first

applied by the trailing motor until the
tape speed falls below 20 ips: at that
point d-c is applied to the trailing motor
to bring the tape to a smooth stop.
The direction sensor indicates which
motor is trailing. With d-c in the motor
field winding the rotor will resist applied
torque even at zero velocity due to the
hysteresis in the rotor. Voltage is never
completely removed from either motor
in order that some tape tension always
be maintained. The end of the tape is
sensed by a photoelectric cell which
receives light through transparent leaders
at each end of the tape. The timing track
is continued on the edges of the 100-foot
transcript so that the control ele-
mont will know when the tape has fallen
below 20 ips as previously described.

The control circuit for one of the motors
is shown in Fig. 3. The transistor, Q-1,
regulates the current through the control
windings of the 3-phase magnetic ampli-
fier, and it switches between saturation
and cutoff at various duty cycles. When
Q-1 is cut off, D-1 conducts, so that the
control winding-time constant is deter-
mined solely by its own inductance and
the 470-ohm resistor. This time constant
is made long enough to prevent abrupt
torque changes and to average the
control current.

Feedback was included to provide close
control of minimum torque. Too much
minimum torque will either allow the
tape to creep or require excessive d-c
holding currents in the trailing motor.
Too little torque will fail to overcome
static friction, and allow a loop of tape
to form. The feedback prevents large
variations in the output current of the
magnetic amplifier which would be
caused by unbalanced line voltage or
small variations in reactor control cur-
cent, especially when the amplifiers are
nearly cut off. The feedback signal is
derived from the sum of currents in all
three motor leads. The diode D-2 limits
the sum output voltage of the current
transformers to 10 volts and thus keeps
the voltage drop across their primaries
negligible under high current conditions.

To generate full torque, one of the other
transistors such as Q-3 is saturated, cut-
ting off the magnetic amplifier control
current independent of the feedback and
allowing full current to flow to the motor.

The direct current which is applied to
the trailing motor when the transport is
slowing to a stop is switched to one
lead of the motor by a relay contact (not
shown on Fig. 3). The d-c flows into that
motor lead and out the other two, back
through the magnetic amplifiers. Al-
though the magnetic amplifiers are biased
into a low torque condition they will pass
the d-c (approximately 1 ampere) since
the average voltage across any one re-
actor must be zero.

**Digital Speed Control**

To determine which motor should re-
ceive full torque, minimum torque, or
d-c, the desired condition of the trans-
port is compared with the existing one.
As shown in Fig. 4, the motion control is
based on a group of speed domains: too
fast (f), faster than controlled (fc), slower
than controlled (sc), and too slow (s).
Various torque commands are shown as a
function of speed and direction for several
desired conditions.

The speed sensing logic is diagrammed
in Fig. 5. The speed is detected by com-
paring the interval between timing pulses
from the tape with the delays of delay
units, as shown in Fig. 6. Two pulses are
generated from a tape timing channel
as it travels over the head, Fig. 6(A) and
(B). The first is used to fire three de-
lay units, two of which, Fig. 6(C) and (F),
establish the boundaries between the
area of usable speeds and too fast or too
slow. The third delay unit, Fig. 6(D),
can be set by the computer to any one of
several delay times representing speeds in
the useful range and provides close speed
control at preset and selectable tape
speeds. It in turn drives a fourth delay
unit, Fig. 6(E), to provide a controlled
zone. In this condition the transport
coasts. The second timing pulse occurs
at a time determined by the speed of the
tape. It is used to sense the condition of
define the speed domain. It is also used to recover before the next "set" pulse. The dotted waveforms in Fig. 6(E) and (F) indicate this resetting when the tape is in the controlled-speed zone. The delay units must be resettable, and the delay time of one must be capable of electronic variation.

Head Assembly Design and Read-Write Method

The 10-track head assembly contains five channels: three information, one timing, and one block mark. Each channel consists of two redundantly paired tracks; the tracks in each pair are nonadjacent to minimize the effect of a speck of dirt lifting a portion of the tape. The timing channel occupies the two outside tracks which are heavily shielded from the interior ones in order that the timing channel may be read while the others are being written.

The timing channel controls tape speed, information density, and the fixed address feature. It assures constant information density regardless of tape speed and makes possible the changing of a single word in a message. Its density must therefore be known and constant. It is permanently recorded, either with a constant-speed capstan temporarily attached or on a separate constant-speed machine.

Read and Write Principles

Since the amplitude of the signal from the tape varies greatly with speed, a system of recording is used that allows the polarity of the flux change to be significant rather than its amplitude. High-gain amplifiers may then be used in which the gain need not be constant. Fig. 7 shows the flux pattern and other waveforms. The idealized timing-track flux pattern consists of 200 complete cycles of flux per inch, or 400-flux reversals per inch, see Fig. 7(A). The timing track read voltage, Fig. 7(B), is the expected derivative waveform from a 0.0005-inch gap looking at a signal of this density. The signal is amplified and squared in a Schmitt circuit, Fig. 7(C); the finite hysteresis of the Schmitt circuit delays the signal slightly as shown. Time pulses are generated from the transitions of the Schmitt circuit: time pulse 0 (TP0) from the negative transitions and time pulse 1 (TP1) from the positive transitions, 7(D) and 7(E). The time pulses must then be slightly delayed, 7(F) and 7(G), so that the information flux pattern may be written in phase with the timing flux pattern. The delay is a function of tape speed and is varied by an analog voltage fed to the delay circuit. The analog voltage is in turn derived from a circuit whose output is a predetermined function of the average frequency of the time pulses fed to it. The flux is laid on the tape in phase with the timing flux so that information may be read or written while the tape is moving in either direction.

The delayed time pulses control the transfer of information to the writing flip-flops. Delayed TP0 transfers the bit to be written to the flip-flop which is controlling write current; delayed TP1 complements the flip-flop. Thus a flux change is written in the center of each line corresponding to the bit to be written; there may or may not be flux changes between the lines. A typical information pattern and resulting ideal flux pattern are shown in Fig. 7(H) and 7(I). The voltage which would be read from this channel during read time is shown in Fig. 7(J). Notice that there is a saturation signal at the center of each line, whereas in between lines there is sometimes a signal and sometimes not. The signal is then amplified more than necessary, Fig. 7(K). The amplifier has enough gain so that one of the redundant tracks may be completely separated from the head by a speck of dirt while a half-amplitude signal is being received from the other track; a saturation signal will still be delivered by the amplifier at the center of the line. The amplifier is strobed by delayed TP1, so that the logic doesn't know what the amplifier output looks like at any other time. The saturation output received at the center of each line with phase-modulated nonreturn-to-zero recording also allows the tape to be read correctly with plenty of amplifier gain margin over a wide range of tape speeds.

Read and Write Circuits

The read-write switch and write circuit for one digit are shown in Fig. 8. During "write," Q4 is cut off and Q3 is saturated. With Q4 cut off, its 10K collector resistor lifts the bases of Q5 and Q6 towards +30, leaving them cut off and the read amplifier disconnected. The silicon diodes at the amplifier input prevent any large voltage excursions from reaching the amplifier. With Q3 saturated, the digit flip-flop will cause either Q1 or Q2 to also be saturated. With the circuit values shown, 15 milliamperes (ma) will flow through the two series-connected tracks and 30 ma through the saturated transistor (Q1 or Q2). The direction of current flow through the tracks is determined by the flip-flop state; i.e., whether Q1 or Q2 is saturated. The read-write switch and write circuit for one digit are shown in Fig. 8. During "write," Q4 is cut off and Q3 is saturated. With Q4 cut off, its 10K collector resistor lifts the bases of Q5 and Q6 towards +30, leaving them cut off and the read amplifier disconnected. The silicon diodes at the amplifier input prevent any large voltage excursions from reaching the amplifier. With Q3 saturated, the digit flip-flop will cause either Q1 or Q2 to also be saturated. With the circuit values shown, 15 milliamperes (ma) will flow through the two series-connected tracks and 30 ma through the saturated transistor (Q1 or Q2). The direction of current flow through the tracks is determined by the flip-flop state; i.e., whether Q1 or Q2 is saturated.
During "read," Q3 is cut off and Q4 is saturated. Q4 takes the full write current through diodes D5 and D6, back biasing diodes D1 through D4. With Q4 saturated, diodes D7 and D8 are back biased, allowing Q5 and Q6 to be saturated, thus connecting the two series-connected tracks to the read amplifier at a d-c level of approximately zero.

Read Amplifier

The read amplifier, Fig. 9, has two difference-amplifier stages and one output stage with more than enough gain to give a saturation output signal at a tape speed of 20 ips. In the first two stages, the common mode gain per stage is less than unity while the difference signal gain is approximately beta. The low common mode gain insures that power supply noise will not be amplified. Each transistor (Q1-Q4) is biased to a constant d-c operating point of approximately 3.8-smitter-collector volts and 1.9-ma collector current. The capacitors shown must only be large enough to have negligible signal attenuation at 20 ips, the lowest tape speed of interest. The lowest frequency signal will be at 20 ips and 100 cycles per inch (all ones or all zeros; see Fig. 7] for a frequency of 2 kc. The highest frequency will be at 920 ips and 200 cycles per inch (all ones or all zeros) for a frequency of 184 kc. The micro-alloy 2N393 transistors have more than enough bandwidth for this application.

The measured current will continue to rise, but more slowly, (B,C) and the slope is now that of R4, (R5 + R6), and the grounded-emitter collector resistance of T1, all in parallel.

Up to this point, T1 has been cut off, but as the collector voltage of T1 rises, so does the base voltage of T2. When T2 begins to conduct, the circuit behavior alters radically. The current through T1 is reduced as the collector voltage of T2 drops, so less current, rather than more, is required from the external source. In fact, as the voltage is increased further, the current required drops to zero and reverses. (C,D,E on Fig. 1(B).) When T1 is completely cut off, the current again begins to rise, and the slope is now R6, R7, and a very large collector resistance all in parallel. At EP = V1, the current crosses the axis and will continue to rise linearly until breakdown.

This negative resistance (NR) curve describes completely the output characteristics of the circuit, just as the plate curves describe a tube. Load lines can be drawn that will indicate loading capability, as will be shown later. In addition it will be shown that the NR curve is an aid in deducing triggering thresholds (duration and amplitude) and switching time.

Derivation of the NR Curve from the Circuit Parameters

It is not necessary to make the previous measurement to arrive at the NR curves for a circuit. Consider Fig. 2(A). Assuming the base swing is small compared to E0, the current through R2 (Ib) is nearly constant at E0/R2. When T1 is saturated, its collector current is (E0/R2) - I0. The drop across the right

References


Kreuder—The Dynamics of Toggle Action

The Dynamics of Toggle Action

NORMAN L. KREUDER
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It is common in the design of regenerative circuits to perfect the d-c (static) design on paper and the a-c (dynamic) design in the laboratory. In the process of working out the static design, a certain amount of engineering judgment can be used so that the resulting circuit will give approximately the required dynamic performance, but rarely will the d-c-designed circuit pass all the performance specifications without some changes dictated by laboratory tests. Although it is awkward to calculate directly the effects of loading and component variation on stability, switching time, and triggering characteristics, it is even more awkward to measure these effects experimentally because interaction of all the components makes it difficult to find the worst combination.

This paper presents a design method using an intermediate step, i.e., the negative resistance curve, between the static and dynamic design. The effects of loading and component variation show up clearly as changes in the negative resistance curves and, in turn, the altered dynamic performance can be calculated easily from these curves.

The method is here applied only to toggle (flip-flop) design, but the extension to monostable circuits in simple. In principle, the method is applicable to other regenerative circuits such as blocking oscillators.

The paper includes the derivation of negative resistance curves from the circuit parameters, a method of evaluating toggle performance from the curves, and an example in the form of a transistor toggle.

Description of the Curve

Fig. 1(A) shows a typical toggle using p-n-p transistors. Suppose the resistor sizes have been chosen to produce some standard swing (V6 to V1) with some standard power supply voltages, (E1 and E2). The object is to evaluate this proposed design.

A variable voltage source is shown connected to one collector, with suitable meters for current and voltage measurements. If the source voltage is either V0 or V1, no current will flow since V0 and V1 are the stable, open-circuit output voltages. Some current will flow at other voltages. When T1 is conducting, and saturated, the current will be zero as voltage very close to zero. If T2 is collector is forced more negative, current will rise rapidly along the saturated collector characteristic, (R0). This is shown as A, B in Fig. 1(B). Since collector current cannot exceed beta, where I0 is the base current, T1 will pull out of saturation when the collector current reaches beta I0.

The measured current will continue to rise, but more slowly, (B,C) and the slope is now that of R1, (R5 + R6), and the ground-emitter collector resistance of T1, all in parallel.

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