IBM Current Mode Transistor Logical Circuits

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The CURRENT mode circuits discussed in this paper and in preceding papers are intended for use in a very large, high-speed digital computer. From the circuit standpoint, this machine could be classed as a mixed synchronous-asynchronous system in which the outputs of chains of logic are often sampled by clock pulses. The system requires circuits which have delays of approximately 20 millimicroseconds per circuit. The basic circuit philosophy discussed here is well suited to the properties of the drift transistor.

Properties of the Transistor

The speed of response of a transistor switching circuit, neglecting stray capacitances, depends on the frequency response and the time constant of base resistance-collector capacitance. Of equal importance is the delay due to minority carrier storage, particularly when this delay approaches the maximum to which one wishes to restrict a circuit. As an example, if one wishes to restrict the circuit delay to 20 millimicroseconds and the saturation delay is 10 millimicroseconds, then only 10 millimicroseconds can be allowed for the transition to the switching threshold of the stages being driven. However, if the saturation delay is eliminated, a full 20 millimicroseconds can be allowed for transition to the switching threshold of the load stages. Clearly, then, a transistor switch operated out of saturation will not have to produce as steep rise or fall times to maintain the same circuit delay as a switch which is driven into saturation.

The frequency response and the collector capacitance are marked functions of the d-c operating point. The situation for a drift transistor is shown in Fig. 1, where curves of constant frequency cutoff and constant collector capacitance are plotted as a function of collector-to-base voltage and collector current. The collector capacitance varies inversely with the 1/3 power of collector voltage, but remains relatively constant as current is varied over a wide range. The contours of constant frequency cutoff bear some resemblance to a family of rectangular hyperbolas. In general, frequency cutoff increases as collector reverse bias is increased. However, for a fixed value of collector voltage, the frequency cutoff will decrease when the current exceeds the optimum value shown in Fig. 1. Also, the frequency cutoff is poor at very low currents.

The curves of Fig. 1 indicate that when a transistor operates on a load line such as x, frequency response and collector capacitance will approach an optimum within the hyperbola of allowable power dissipation. The disadvantage of this load line is that, when on, the transistor is required to dissipate more standby power than would be required with a load line that extended into the saturation region.

Basic Current Mode Switch

Consider the basic current mode switches shown in Fig. 2. The circuits are differential amplifiers with one input reference to ground in the p-n-p circuit, and -6.0 volts in the p-n-p circuit. The input signal to the top transistor, \( T_1 \), swings about ground, but only by an amount sufficient to switch current completely into either transistor \( T_1 \) or \( T_2 \).

In the p-n-p circuit of Fig. 2 the top transistor, \( T_1 \), is off when the input potential is at +0.4 volts and the bottom transistor, \( T_2 \), is conducting. When the input potential is at -0.4 volts, the bottom transistor is biased off and the top transistor conducts. Since the potential changes at the input are very small the 910-ohm resistor and the +6-volt supply constitute a constant current source, and there is little difference in the current supplied to the top or bottom transistors. The output signal is developed across the 240-ohm load resistor returned to -6 volts. In order to make the output signal swing about -6.0 volts, a small current bias is added through the 2.45K resistor returned to -12 volts. With this arrangement, the output potential varies from off value of -6.4 volts to an on value of -5.6 volts.

The p-n-p circuit of Fig. 2 has an input referenced to ground, and outputs referenced to -6 volts. Because of the 6-volt difference between input and output, a p-n-p switch cannot drive another p-n-p

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Fig. 1. Drift transistor characteristics

Fig. 2. Basic current switches

Fig. 3. Noise problems

Fig. 4. Current switching "and" and "or" circuits

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The optimum transistor was necessary because the optimum of 4.4 milliamperes shown in the input should be switched than the transistor driven and the stray capacitance. Rather than the input capacitance of the stages being through which the operating point must pass as the transistor is turned on or off, the operating point is always closed to a region of good frequency response and low collector susceptibility of the circuit. When the load network is located close to the stages being driven, the basic current mode switch is not susceptible to power supply noise. Three possible noise generators are shown in Fig. 3. First, a noise generator is inserted between the -6.0-volt reference supply and the load to represent noise on the -6-volt supply. Because of the ratio of the resistors in the coupling network (2.45K to 240 ohm), virtually all of the noise voltage will be applied to the base of the top transistor as well as to the base of the bottom transistor. When the noise is applied in this manner, it will cause little trouble, because the circuit is a differential amplifier, and switching can be accomplished only by changing the potential of one base with respect to the other. Noise on the collector bias and the emitter source supplies (12 volts and +6 volts) will have to be of large amplitude to cause trouble, since these supplies are separated from the circuit by large resistors that join the circuit at points of low impedance.

Inductive coupling, which might come from adjacent signal wires and which is represented by the noise current generator in Fig. 3, is not troublesome. This is because the basic current mode switch presents a high output impedance in the loop through which any inductively coupled noise current must flow.

Of the three noise situations shown in Fig. 3, the problem of capacitively coupled noise from adjacent signal wires, represented by the voltage noise generator and the signal wire capacitance, is the most critical. This is not serious, because the input node has a low impedance (220 ohms). One modification which will make the circuit more sensitive to noise is the inclusion of a peaking coil in the coupling network in series with the 240-ohm load resistor. The peaking coil will raise the node impedance, and capacitive coupling from adjacent wires will be more of a problem. Also, the peaking coil will act as a low pass filter in series with noise generator, and the differential amplifier property of the circuit will be decreased.

**Logic Circuits**

By providing additional transistors, the basic current switch of Fig. 2 may be extended to perform logic. Two logical circuits capable of performing the "and, or, and inversion" connectives are shown in Fig. 4. For this discussion, a binary "one" is defined to be the most positive input to a switch regardless of whether the signal in question is referenced to ground or -6.0 volts. One logical feature of current mode circuits can be seen in Fig. 4. That is, there are two logical outputs and they are complements of each other. As

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a logical "one" is defined here, the top outputs are inverted and the bottom outputs are normal. The fact that inverted outputs are always available eliminates the need for a separate inverter building block in a system. In a long chain of logic where inversion is frequently required, the result is a reduction in over-all delay.

The two logical circuits of Fig. 4 will generate the necessary logical connectives required in a system. However, a separate "exclusive or" building block would be an advantage, since three of the logical blocks of Fig. 4 would be required to generate the "exclusive or" statement and also there would be a delay of two logical blocks in cascade involved. The simple arrangement of logical blocks shown in Fig. 5 will generate an "exclusive or" statement with a delay of only one logical block. Only the p-n-p version of the circuit shown, but the n-p-n version can be formed in a similar manner. The "exclusive or" circuit consists of two parallel "and" circuits which generate \( A \cdot \overline{B} \) and \( \overline{A} \cdot B \). With the four inputs connected as shown, only one of the "and" circuit outputs can be connected to form the "or" circuit required to complete the "exclusive or" function. Under the input conditions \( A \cdot \overline{B} \) or \( \overline{A} \cdot B \), the inverted outputs of both "and" circuits will be conducting and two units of current will flow into the load network. This network is designed to give a normal output only when both sides are conducting, and in this manner the inverted "exclusive or" statement is obtained. The inverted outputs will supply only one unit of current when the normal "exclusive or" inputs \( (A \cdot \overline{B} + \overline{A} \cdot B) \) are present. However, because of the special coupling network, the output signal will not be large enough to switch the load stages. The "exclusive or" circuit requires both the normal and complemented input signals. This is no problem, since both normal and complemented outputs will always be available from the driving sources.

No discussion of a set of switching circuits for a computer would be complete without reference to some means of storage and some means of generating a well-defined pulse. The storage circuit in this case is shown in Fig. 6. It consists of two basic switches cross-coupled to form a symmetrical bistable flip-flop. The flip-flop can be set in either position through the pull-over transistors on either side. An "or" function can be built into the flip-flop by paralleling the pull-over transistors. Operation is in no way different from the logical block circuits of Fig. 4, previously described.

A basic current mode single-shot is shown in Fig. 7. The circuit again consists of two basic switches cross-coupled together, but in this case one side is through a short-circuited delay line. The bottom n-p-n transistor is biased off by the network at its base. The short-circuited delay line is terminated at the sending end, and the pulse width at the output is determined almost entirely by the time required for the wave front at the delay line input to travel down and then back up the delay line.

In any computing systems, situations are encountered where it is necessary to drive loads located at a considerable distance from the driving source. This may be done by driving conventional coaxial transmission line and terminating the coaxial line with either of the circuits shown in Fig. 8. Both the arrangements shown here are driven by a basic current switch. The n-p-n line terminator at the top of Fig. 8 is a Class A grounded-base amplifier. When the top output of the basic switch driving the line is off, the n-p-n transistor conducts and approximately 6.5 milliamperes flow into the current sink formed by the 660-ohm resistor and the -12.0-volt supply. When the top transistor conducts, the emitter current of the n-p-n grounded-base stage is reduced to 0.5 milliampere. The input impedance of this stage has a small inductive component and an impedance of 11 ohms. The 82-ohm resistor is added to increase the total impedance to 93 ohms and match the characteristic impedance of the coaxial line. The small capacitor compensates for the inductive input component. The value of the series resistance can be changed to match lines of different characteristic impedance if desired. The p-n-p line terminator at the bottom of Fig. 8 operates in the same manner. In this circuit the base is biased to -3.0 volts so that the output signal will be referenced to -6.0 volts. The n-p-n circuit differs from the p-n-p circuit in that it translates the output of the basic p-n-p switch from -6.0 volts up to ground level. Because of this, the n-p-n grounded base amplifier can also be used as a coupling means between two p-n-p logical blocks.

In concluding the discussion of the basic circuits, reference should be made to the component tolerances used in the design and the speed of operation that has been achieved with these circuits. Some design information will now be summarized.

Power supplies .... ±4%
Resistors ....... ±3%
Transistors ....... 70 megacycles \( \leq f_t \leq 150 \) megacycles
5 micromicrofarad \( \leq C_e \leq 1.5 \) micromicrofarad
40 ohms \( \leq r_e \leq 80 \) ohms
Emitter base breakdown .... > 2.5 volts

Circuit delays range from 6.0 to 22 millimicroseconds, the longer delays being associated with the larger loads. The basic logical block is designed to have a fan-out of 3 bases. The number of logical inputs is dependent on the number of loads. Maximum inputs are: 6 inputs for a load of three bases, 8 inputs for a load of two bases, and 10 inputs for a load of 1 base. In general, circuit delays are a function of the load and are not greatly affected by the number of logical inputs.

References
Discussion

T. R. Finch: The selection of a logical circuit for digital systems reminds me, in some aspects, of the procedure that a family goes through in selecting trees for the new one-acre lot. The house is located on a very barren plot, and since they would like to grow their investment, they decide to buy some trees, and, of course, they want to get their money’s worth. Well, they can invest in some evergreens which are very glamorous and present a very spectacular show throughout the year. Depending on where they live and the climate, in a number of years they may be able to call their little one-acre plot their dream place. However, they had better give some serious consideration to the root structure and soil as well as to the glamor above ground if they are indeed to enhance their investment.

I think to a certain extent the design of large-scale systems involves similar problems. It is fun and pleasant to design a glamorous circuit with many storage elements. Sometimes we cannot understand exactly how they operate, but they operate like a “whizz-bang” system.

Companies that have been in the computer business for a long time, have to balance off system requirements and bring into being a system that has system efficacy. If there is available a whizz-bang system control and calculator that operates at 100-megacycles but must stand around for an hour and wait for the peripheral equipment to perform its data-processing task, then the system efficacy and low cost are most likely imaginary. What we are interested in is the integrated job of reliability at the least cost.

Transistor resistor logic (TRL) is not a glamorous circuit. It is just a “work-horse” circuit that gives you a good deal for your money. I think that the TRL circuit designer lives up to his responsibilities of providing a basic circuit that can be understood, has a high amount of flexibility and low cost are most likely imaginable. What we are interested in is the integrated job of reliability at the least cost.

Another point on which I would like to comment is how we view the use of the transistor as a logical element as opposed to the use of another device in this application. This really depends upon the size of the system, reliability, and cost primarily. (We believe that in the end almost all characteristics, including reliability, have to be priced out.)

At this meeting we have seen circuits which use transistors for logical input, other circuits which use diodes for logical input, and TRL which uses resistors for logical input. We believe that resistors, given the same selection that semiconductors will be given, will prove more reliable and more economical and will justify their use wherever speed is not completely dominant.

My basic contention is that people who are using transistors for each logical function are indulging in “rich living,” and they have got to get something out of it. What do you get out of it? In current mode switching you get speed. With direct coupled transistor logic (DCTL), you get simplicity and I contend that at the present time this is not enough to offset stiff transistor requirements and inadequate protection against sporadic error. However, I think that DCTL should be commended; it has been a real catalyst since its circuit simplicity has triggered more rapid evolution of digital systems employing simple logical circuits. I think now is the time to leave DCTL because of the problems related to the severe requirements on the transistors. As time goes on, there are severe requirements on systems, and the transistor is used for logical input it is going to be an expensive system.

In TRL, I think that there is a balance, a flexible balance, that permits the logical designer to meet the system’s engineering needs. A study has been made to determine the efficacy of a complete integrated system that places speed requirements on various blocks, sorters, and calculators, input-output stores, etc., and the study resulted in a group of equivalent logical speed. Once the speed requirements on the circuit are set, what do you want to optimize? The answer is the economics because reliability, maintenance, and the first cost of designability all have priced out.

The design of TRL circuits is flexible and permits a variety of speeds. Given a year or two, the diffusion-type devices are going to move the alloys out of business, and you will be able to obtain, for the same amount of money, diffusion-type devices of high-speed low-capacity reproducibility and reliability. Our premise in TRL is that it is a good bet to take advantage of what is going to be offered.

As to our thinking in regard to bringing a system into being a couple of years from now, we are betting on the diffusion-type devices with a simple circuit that we can understand, and use this in large numbers. We can realize our speed requirements, and we can obtain the various economics from the simple circuit by just scaling the impedance level up or down. This gives us the desirable degree of protection against malfunction. If we want to go to higher speed we just lower the impedance level at the inner-stage, and we get high speed with some sacrifice of logical rules, or else we have to use more power.

Our premise again is that d-c power, as it has been refined throughout the years, is the best buy that you can get. You should invest in d-c power in many cases, although there is an increasing use for air-borne applications. I think, if you wanted to design restricted, small scale special-purpose air-borne computers, you would get most value from carefully designed TRL circuits: low power, low power consumption, and operation on low voltage.

I do not think that I would use TRL if I had a real time problem on a time-sharing basis where I had to get down to milliseconds per second. I do not know what I would use for sure, but I might just have to use some of the transistor rich living I mentioned. I have great confidence in the performance of diffused junction transistors, and I am not afraid to use them, but I do think that it is going to be some time before they are as cheap and as reliable as resistors. We believe the same is true for diodes. With the same care and attention given to the fabrication of all devices, I think that the resistor is going to outstrip the diode and transistor for a long time to come.

James B. Angell: I have one disadvantage in arguing with Mr. Finch, in that basically I am speaking of DCTL predicated on experience. This is not just new and glamorous; we have had experience with it. To some extent what he said and others, in fact, will say about DCTL must be based on a fair amount both of design and actual usage and experience.

Before I go on with other comments, I would first like to augment to some extent the question of cost consideration that Mr. Finch started. This is that it is not really the cost per logical element which is of primary consideration in any computer, but it is rather the cost of, or per, logical decision. Certainly there are some cases where there are real time problems with a time scale of doing decisions sufficiently slow so that we are not primarily concerned with how many computations you can do per second. It is true throughout the majority of cases, if you can do the job faster, you can do it with fewer elements. You are not necessarily going to come out with the conclusion that DCTL is faster. I merely wish to augment Mr. Finch’s thought.

What is the primary concern? What does it cost to make a given decision? DCTL is certainly not one of the faster types of circuit. It is roughly comparable in speed with what is called resistor-capacitor coupled transistor logic (RCTL), I believe.

This brings us to another point regarding cost. At least in the case of a limited number of machines a very strong factor in the cost is the designability of the circuit. That is, how easy it is to go from paper designs up to the final layout of the machine. I do not know this fact in the case of transistor resistor logic, but in DCTL I know that it is relatively straightforward. This circuitry can be compared almost to a relay logic circuit when you consider each relay to be of single-pole, monophase arrangement. The transistor is single-pole, single-throw relay, with, unfortunately, a connection between input and output. Nevertheless, the transformation from original layout to final machine is relatively straightforward once the original layout has been designed on the basis of simple logical rules.

Again with regard to cost, to do a given job in a given length of time with the slowest possible circuit will require less time, and it has been found by experience with DCTL, and in various other cases, that reliability is not only on the basis of components, but also on the basis of interconnection of the components. How many nodes you have in the circuit becomes quite important; the total number of contacts, the total number of gadgets, if you will, that you can put in conveniently on a given panel. I add this point to indicate that there is indeed something to be considered not only from the standpoint of a minimum number of circuits, but also for doing a given job in a given length of time.

Factor to be considered is that of minimum component count. Minimizing the number of costly components does not
necessarily make for minimum over-all cost. It has been experienced and stated by one of the organizations that has been involved with DCTL that the over-all cost of a DCTL machine is not much more than the cost of an RCTL machine of equivalent capacity. Furthermore, it will require less design time because of the simplicity of the design and the smaller number of actual components to be determined.

Finally, I would like to leave you with the thought that the logic described by Mr. Walsh is a complementary version of DCTL, in that both use transistor logic.

R. H. Baker: I do not think that basically there is any difference between the circuitry that we can argue about, but for the sake of discussion I will make comments about it.

First of all, let me consider my own circuitry. On one hand the cost of the components is expensive, but on the other hand if we can estimate 75 man-years for doing a job we save 30 kilo-dollars per man year, which is about what one does in a research laboratory. Then this is more than the total cost of all the parts of the machine that we were to build, and for this research job I do not see how we could have done it any other way. Our goal here is to build something for a system evaluation. I do think, however, that the cost of the components will go down, and that this circuitry of ours will become simpler and cheaper. It does have a high-performance record, and as time goes on it can be made simpler.

Now I would like to ask a question about TRL. To show no favoritism I will agree that resistors are more reliable than diodes, and if you can say that reliability is measured by how much per cent something changes, then a resistor changes less percentage-wise than a diode does. On the other hand, there is a real question with the greater variation that you can stand with the diode than you can with the resistor because the latter does consume part of the margin of linear devices. I do not at all see that, with the greater allowable variation of diodes, that resistors offer a truly more reliable way. I also say that a hermetically sealed resistor (but it would be expensive) would be very effective.

I also want to point out that the designs of a paper machine are nothing like getting a machine to work. I think that some of the transient problems are the ones that are going to be really hard to solve, not the d-c problems in TRL. The problem is: One has a machine designed on paper, and you build it up and run a program through it to see if certain parts of the program work. This is usually the type of error where you must allow yourself enough flexibility to overcome the difficulties once you have started running the machine.

With regard to DCTL, I just cannot believe that a 3-terminal device is going to be as reliable as a 2-terminal device. I think the diode is more reliable than a transistor because a diode is governed by a bulk phenomenon than is a transistor, hence, the transistor is more amenable to surface conditions affecting it than is a diode. I think that the same comment is true of the circuity described by Mr. Walsh. I think that a diode per logical input is expensive. On the other hand, I do not think that he expects this to last very long. In our position, we do not have to have something planned 5 years ahead, and this is where we differ basically from IBM, where the use is commercial as well as military. I think that by the time we go to his type of logic there will probably be something out with a little faster speed which will put diode logic definitely out of business. I think that it will probably be a different type of device produced by companies such as Radio Corporation of America, with three and four leads.

J. L. Walsh: I find it hard to speak in rebuttal since our problems are different than, for instance, the areas in which Mr. Finch operates. I have no argument with resistor logic, and I can certainly see that in many slow-speed applications it is economically worthwhile.

The advent of the drift transistor has opened up new areas of real high-speed operations, and here I do feel that saturation techniques will not be adequate. We will not in the future be able to neglect the ultimate storage delay which might be 5 or 4 or 3 millimicroseconds.

Chairman Felker: I have a series of questions to present to our speakers. The first question comes from H. J. Gauss, University of California in Los Angeles, for Mr. Finch: “Could not a gain in speed be obtained by the use of diode clamps to limit swings, and thus prevent saturation?”

T. R. Finch: Yes. This is a common way to operate and to use more power and what I call a “speed-up configuration.” I commented on this when I pointed out that for a large number of applications falling in the fields of industrial control or business automation, the basic simple circuits with modern-day junction transistors will meet speed-up requirements without resorting to clamps for nonsaturation arrangements.

Chairman Felker: The next question is also from Mr. Gauss, for Mr. Angell: “Could not the “hoggling” of current by one of several paralleled bases be minimized by the use of series resistors?”

J. B. Angell: First of all, to minimize hoggling, the manufacturers of transistors put in what is called “a base spreading resistance.” This is not very well controlled, and indeed it has had some effect.

On the question of hoggling, it is fairly stable with time so that if you have a transistor that meets the specifications initially, it will continue to meet that characteristic, not one of age. To add such a base resistance does indeed slow down the turnoff of the transistor. If you will recall Fig. I of my paper, when the first transistor is activated the second one is supposed to go off. The higher the base resistance of the transistor going off, the slower it turns off, until eventually it gets as bad as TRL. Of course, by adding the resistor you are adding an additional node. Experience has shown in general that when a circuit has relied on transistors to avoid hoggling, it has been adequately successful, at least to date.

T. R. Finch: I wish to comment on Mr. Baker’s comparison of DCTL to a degenerate type of DCTL. This is definitely not the case because the big problem of DCTL is in its lack of adequate protection against malfunction resulting from a forward-biased off transistor, which is one of the strong differences between DCTL and TRL.

Chairman Felker: From A. Wenstrom, Hughes Aircraft, for Mr. Baker: “Is diode recovery a serious problem in your high-speed circuits? What diode type do you use?”

R. H. Baker: Yes, it is a problem. However, I would like to point out that one manufacturer is now making a fairly fast diode. Although it was not meant to be particularly fast, if you are really after speed, you can get several manufacturers today within a year that will have recovery time in the order of a millimicrosecond.

Chairman Felker: This question is addressed to Mr. Baker and Mr. Walsh, from S. Disson, Burroughs: “Please comment on pulse propagation problems in circuits with 5- to 30-millimicroseconds stage-delay characteristics, particularly on when and why coax is necessary. Also would Mr. Baker please comment on susceptibility of his circuits to coupled noise?”

J. L. Walsh: I think we gain when we use coaxial for cable that goes beyond 3 feet: below that, down to 8 inches, we use twisted wire. Beyond that, as far as propagation time, you have to keep track of the delay in the coaxial cable.

R. H. Baker: We do not know the answer to this question; this is what we are working on. We have a feeling that coax is not the answer because it makes the machine too big. It seems to me that if you are going to make the machine run fast, it is going to have to be small to keep the propagation time down. The only way to do this, I think, is to invent a new package where everything stays close to the ground plane. I do not think that there is a simple, general solution to this. All that I can say at the present time is that we have potential designs, and we are trying to get a solution.

Chairman Felker: This is for each panelist, and is from J. C. Hawkins, ALWAC: “Mr. Baker gave a comparison of 20,000 transistors and 40,000 diodes for one machine. Would other panelists comment on, or estimate the number of components required for typical general-purpose computers using the type of circuits described?”

T. R. Finch: We made a comparison for a part of our system using about 7,500 TRL circuits. The difficulty here is that we worked to the needs of a system, an engineering analysis of what the blocks had to do in the way of terminal speed, if we came up with a solution that was faster it had little value unless the component count was reduced. The prime, dominant characteristic of Mr. Baker’s circuit is to use more components to get speed. His circuits are more complex than ours, so the comparison was made with DCTL. From our analysis it looked as if DCTL ran from 2 to 1.5 to 1 greater in transistor count, and costing joints and cost place of transistors and transistors. Our estimate for the block, as of 1958 and of 1962 both, was that the
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TRL was 2½ to 1 less expensive for the same speed performance in the block.

Chairman Felker: Mr. Hawkins asks, "I believe that you stated that you had 34,000 transistors. How much would that be?"

T. R. Finch: Twenty thousand transistors, and no appreciable number of diodes, and we are averaging about five resistors per transistor.

Chairman Felker: Do you have some figures on that, Mr. Walsh?

J. L. Walsh: I would not care to compare numbers with numbers used in TRL machines, as compared with the other numbers discussed here. Frankly, the comparison would be relatively favorable, but I do not think that the machines were designed to do the same job. I think it would be quite meaningless to point out what order of numbers has been used in TRL machines.

Chairman Felker: Here is a question from D. Weisser, IBM, for Mr. Baker: "Do you make any effort to select transistors for minimum minority carrier storage?"

R. H. Baker: The answer to this is, "No." With later-type transistors that we are working with now, storage is practically nonexistent.

Chairman Felker: We now have a question posed to all speakers from Louis Kurkjian, Hughes Aircraft: "Which of the 4 systems described are more applicable to synchronous and asynchronous operation?"

J. L. Walsh: I think that the system I described is applicable to either synchronous or asynchronous operation, but certainly there is less of a problem at high speed if you run equipment as synchronous.

Chairman Felker: I do not see why any of these circuits could not be used in both types of machines.

James B. Angell: DCTL is used almost completely in asynchronous machines.

T. R. Finch: All systems somewhere must be synchronized. As far as TRL is concerned, you wait for it to propagate and set up on registers, and then it is clocked out.

Chairman Felker: R. K. Richards, Consulting Engineer, asks of all speakers: "With all the virtues of the transistor circuits you have described, how do you account for the fact that existing tube computers are not experiencing competition from corresponding transistor computers?"

J. L. Walsh: I would be happy to answer that one. The existing tube computers are not really competitive from the standpoint of the ultimate use to be achieved. I think that most people are not designing replacements, but rather are designing equipment to do other bigger jobs faster.

Chairman Felker: The fact is that every-one is planning a transistor computer. I do not believe anyone is planning new vacuum-tube machines. I would expect that in 5 years most of the computers will be transistor based. In the military field transistors have pretty well won out competitively.

James B. Angell: There is no doubt about it.

J. L. Walsh: I would like to make another comment on that fact. Until we get a vacuum tube that has a diode drop equal to the diode drop of the transistors, I think that the transistor will be pretty difficult to beat for high-speed operation.

T. R. Finch: There is a comment I would like to add. It is difficult to supersede quickly a system implementation that has been refined for over 40 years.

Chairman Felker: This next question comes from O. S. Goda, Collins Radio Company, and is addressed to Mr. Finch: 'Transistors 2N393 and 2N591 are relatively expensive devices at $7.50. How do you justify economy when 0.25-microsecond propagation time is obtainable with a diode or-transistor nor circuit using alloy-junction 8-megacycle, $1.50 transistor?'

T. R. Finch: If I had to bring into being next month a large-scale system, and it would be the only system I was going to design and put to work, then I think that the comment is well founded. I made the point that we were investing in the future, and that future is that the diffused-junction transistor, within a reasonable time on the order of 2 years, is going to be less costly, easier to make, and high speed. Beyond a period of 2 to 4 years I would question that you will be seeing many alloys around in a new system.

Chairman Felker: This question is for Mr. Angell, and comes from C. E. Baker, McDonnell Aircraft: "Exactly what does the increased number of transistors of DCTL, as compared to TRL, buy in the way of speed, reliability, and complexity?"

James B. Angell: In terms of speed for a given transistor, I would expect that the ratio is something like two; that is, DCTL is between one and two times faster. What it buys in the way of reliability, I cannot say.

In complexity I think, without question, that there are slightly fewer nodes using DCTL because each element in DCTL is an active element with gain. You do not require occasional inverters or transistors to reinstate the loss you have had in the dissipating elements. Each element is active in this case.

R. H. Baker: In other words, they are both slow.

Chairman Felker: The next question is from L. P. Retzinger, Litton Industries, for Mr. Baker: "Do any oscillation problems arise from using emitter followers in logic?"

R. H. Baker: There definitely are, if you use followers in a row without isolating the diodes.

Chairman Felker: Mr. Retzinger also asks Mr. Finch: "Do you place a restriction on max-$\beta$, since storage time is a function of excess base current?"

T. R. Finch: We have debated about doing this, but we have not done so, so far. We're using the devices that I have been using, the microalloys and the microalloy diffused base, the requirements on the transistors are a minimum, d-c beta of 40 collector current of 5 mils with a possible 'on' voltage of 125 millivolts. The worse worse computation we have programmed on our computer, as I have shown you, did not put restriction on beta and included devices with d-c beta exceeding 100. I do think that we would get improved logical rules if we did.

Chairman Felker: Here is a question from W. Libaw, Magnavox Research Laboratories: "Do you use a pulse to trigger flip-flops? If so, is there a problem of gating the 'old' state of the flip-flop with the clock pulse?"

T. R. Finch: The way we are operating so far is straight d-c level. Although we are not treating the flip-flop any differently than a d-c logic stage, we have been giving consideration, as one might expect, to capacitive-coupled flip-flops. I mentioned that the basic d-c level logic circuit covers the order of 90 per cent of logical needs, with the larger part of the remaining 10 per cent in the control circuit. Special pulse triggers were not used for the speeds described.

Chairman Felker: Here is a question from W. Woods, RCA, for Mr. Finch: "In calculating the performance curves for TRL circuits, what specifications are assumed for minority-carrier storage, and how well can this characteristic be controlled in practice?"

T. R. Finch: Minority carrier storage effects are controlled by 1. transistor design in regard to lifetime of storage bodies and the volumes of these bodies, 2. the depth of saturation due to forward drive, and 3. the sweep out reverse current. Since we were primarily interested in the worst-worst performance, we placed requirements on the transistor turn off under our most severe logical conditions, in our case, 5 active inputs before turn off, and minimum available sweep out current. The forced beta became about 3, and the minimum allowable turn off time for the 2N393 was specified as 0.35 microsecond. Under these conditions, it was not unusual to find delay variations ranging down to less than half of the specified maximum.
MICROSDIC is a data acquisition and handling system. It is, therefore, the link between the test object and the electronic computer in an advanced scientific or technical study. Fig. 1 shows the cabinet which contains the central data processing electronics of the MicroSDIC system. It contains the data sources for time and selectable title constants. It also contains the commutators, the digitizer, the central program unit, and a power supply. Data are coming in through transducers from the test directly or through frequency modulated-pulse duration modulation (FM-PDM) radio link through telemetering equipment. The MicroSDIC output is usually magnetic tape. The tape unit is of the same size as the unit shown in Fig. 1. The MicroSDIC meets the need for high speed in data processing, high accuracy, compatibility with all standard computers, reliability, and outstanding flexibility. Its design for universal use allows the build-up of a variety of complete data handling systems. The following paragraphs will show how these characteristics are achieved. Special attention is given to the characteristic of flexibility which makes it possible for the MicroSDIC to create basically different data output formats as required for different computers with their contrasts in format and input specifications.

Data Sequencing and Coding

The operation of the over-all system is illustrated by Fig. 2. The test object may be a missile, a windtunnel model, a power engine, a chemical plant, or any other complex system. The transducers feeding the MicroSDIC system provide electrical signals proportional to the test values. Examples of the great variety of these are pressure, temperature, stress, and angle of attack. Two different types of test have to be considered, the air-borne test and the ground test.

In case of an air-borne test, see Fig. 3, the transducer outputs may be fed into an air-borne commutator. This switching device sequences the data and feeds its output into the air-borne signal converter. The air-borne signal transmission normally use pdm and FM modulations. A ground station records such signals on magnetic tape. The tapes are brought into the test center and played back into a demodulator. The demodulator provides straight pdm outputs for a pdm digitizer. It also demodulates the FM signals into amplitude modulated (AM) signals. Another MicroSDIC digitizer converts these signals into digital data in the desired code. The operation is simpler in the normal ground test, (see Fig. 4). In that case the analog transducer outputs are given to a standard commutator which feeds directly into the analog digitizer.

Digital transducer outputs are also brought to a commutator. Thereby, the sequence of their recording is controlled. This sequence is important since the later computer program has to be established on this order in the incoming data flow. In Fig. 5 note how the different data sources feed into the central program unit. The pdm digitizer had been mentioned before. The commutator for analog signals is connected to the digitizer which feeds into the programmer.

Another data source is the time information. Most tests are of the "dynamic" type and, therefore, require time information for each data point. Static tests make use of the time unit for counting test points and other purposes. There are also switch combinations which give digital constants and may be used for test identification (date) or special computer information (program selection).

In summary, then, there are five digital data types:

1. Constants.
2. Counter output from time accumulator or decoder.
3. Digitized data from the analog digitizer.
4. Other data.
   (a). From the subcommutator for digital inputs.
   (b). From the PDM digitizer.

Types 4(a) and 4(b) will not normally be used together. Therefore, normal MicroSDIC build-ups use four types of data. The sequence within each group is determined by the commutator and the code is determined by the digitizer. Straight binary or binary-coded decimal are mostly preferred. The sb/bed translator in Fig. 5 is used in cases where both codes are wanted simultaneously. It might also be that the general system is selected to be straight binary but that for a special test bed output is wanted.

The translator is based on the "doubling" principle. The numbers are serially shifted from an sb register into a bed

Fig. 1. Basic MicroSDIC cabinet

Fig. 2. MicroSDIC system, block diagram

Fig. 3. MicroSDIC inputs for air-borne tests

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Schwab—MicroSDIC, A High-Speed System

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