switching circuits by a substantially smaller number of components and connections, and by extremely-low power consumption. Circuit simplicity and low dissipation are obtained at the price of limited gain, small voltage swings, and a comparatively low upper limit on internal temperature. Rather severe requirements on transistor parameters, particularly input impedance and saturation voltage, are compensated by almost negligible dissipation and maximum voltage requirements. The total cost using DCTL is comparable with other techniques, because the tightly specified transistor eliminates considerable complexity in system design and manufacture.

References

Symmetrical Transistor Logic

R. H. BAKER
NONMEMBER AIEEE

THIS paper discusses symmetrical transistor switching circuit techniques. The circuitry is designated "symmetrical circuits" because the basic circuits employ both p-n-p and n-p-n transistors in approximately equal numbers which result in networks that exhibit a high degree of operational and topological symmetry. The major practical advantage of this circuitry over other types lies in the ease with which basic circuits may be integrated into a digital system. This advantage is made possible through 1, keeping the circuit configurations flexible to satisfy many different system applications, 2, worst-case circuit design with regard to component stability and system loading requirements, 3, use of only standard commercially available components, and 4, insisting that all present-day circuit designs be applicable to known future device trends. The major criticisms of the symmetrical circuit techniques is that the circuits require a greater number of components for a specific equipment than do other types of circuitry because they can be engineered to build the specific system. However, it is felt that this criticism is not justified in this case for two reasons. They are: 1, The additional cost of components required for symmetrical logic is more than counterbalanced by the shorter system realization time required. This is particularly true for an establishment, such as the Massachusetts Institute of Technology Lincoln Laboratory, that is engaged in system research and development. And, 2, that symmetrical logic techniques are more adaptable to future developments in the device, circuits and system area than other types of circuit logic.

It is the purpose of this paper to show why, when, and under what conditions symmetrical circuit techniques should be used, along with probable future developments, through the discussion of the circuit techniques and relating their circuit capabilities to the solution of system problems.

I. Basic System Requirements

A. Initial

The initial specific system for which the symmetrical circuit approach was intended had the following requirements:

1. General-purpose computer applicable to real time problem solution.
2. All solid-state machine.
3. Nonairconditioned ground environment.
4. Synchronous machine with a basic clock rate of 3 microseconds, (μs).
5. Memory capacity of 8,192 registers, 28 bits in length, with a memory cycle time of 6 μs.
6. Semiportable housing.
7. Minimum conception to completion time with a minimum of staff.
8. Maximum reliability with minimum maintenance.

B. Additional

It was also the goal of the circuit designer to build circuitry that was sufficiently flexible to meet requirements for all other ground-based digital-data processing systems contemplated at the time (there were several).

II. Basic Circuit Modules

A. General Comments

Aside from the general system requirements of Section I, there are several other component-circuit-system requirements worthy of special note. They are:

1. That the circuits require minimum specification components (single-ended specifications when possible).
2. That all components be commercially available stock items.
3. That the circuit techniques be sufficiently flexible to incorporate future higher performance devices to satisfy future needs.

References

Fig. 1 (right).
Symmetrical buffer inverter
higher-performance system requirements that may be needed.

4. That the circuit designs concentrate on fundamental device-network-system principles, thereby pointing out future trends in these areas and furthering the state of the art.

B. BUFFER INVERTER

With the aforementioned system and circuit requirements in mind and considering the transistor field as it existed in 1955, it seemed advisable to utilize p-n-p transistors to generate fast "positive-going" transients and n-p-n transistors to generate fast "negative-going" transients. This was first done in the form of a buffer inverter shown in Fig. 1. Some of the salient features of the circuit shown in Fig. 1 are:

1. Each transistor has positive base current applied while in the off condition and the numerical value of this current is equal to \( \Delta V/R_b \).

2. Resistor values \( R \) and \( R_b \) along with \( \Delta V \) may be chosen to yield a small uncertainty region (\( V_u \)). \( V_u \) may be centered around ground or shifted up or down over a large range.

3. \( R_L \) is merely a standby resistor and therefore can be almost any value.

4. The circuit is current demand, that is, it draws current (power) from the supplies in accordance with the load requirements.

5. The circuit power gain is approximately equal to \( \beta \) (grounded emitter transistor current gain), i.e.,

\[
\beta = \frac{P_{out}}{P_{in}} = \frac{2\alpha I_e}{2\alpha I + 4\alpha I} = \frac{2\alpha I}{2\alpha I + 4\alpha I}
\]

6. The circuit is fast. This is so because transistor hole-electron storage effects are minimized.

7. The transistor specifications are not critical.

8. The circuit has high utility and is flexible, i.e., the circuit may be: (a) used with any supply voltage within reason (note! Not necessarily equal positive and negative supplies), (b) designed with different values of \( R \) and \( R_b \) for the p-n-p and n-p-n to accommodate nonsymmetrical loads; (c) used with different-type transistors to create unusual circuit effects, etc.

C. FLIP-FLOP

D-C Considerations

Two buffer inverters of the type shown in Fig. 1 may be connected together to form a symmetrical flip-flop as shown in Fig. 2.

The d-c considerations of this circuit are the same as for the buffer inverter previously discussed. However it is worthwhile to point out that the ratio of total power drain on the supplies to the power delivery at the output terminals is almost unity, i.e.,

\[
P_{out} = P_{supply} = \frac{P_{out}}{P_{supply}} = \frac{2\alpha I_e}{2\alpha I + 4\alpha I}
\]

where \( I_e = I \beta \) then

\[
P_{out} = \frac{2\alpha I}{2\alpha I + 4\alpha I} = \frac{1}{1 + 2/\beta}
\]

\[\text{efficiency}\]

Transient Considerations

The important transient considerations of the symmetrical flip-flop may be seen with the aid of Fig. 3.

Salient points to note about the transient behavior of the network are:

1. The hole storage of the saturated transistor is minimized because large current is drawn from its collector during the storage time, thus clearing out the stored minority carriers quickly.

2. The rise and fall times, of the output, after the storage time is directly related to the ability of the conducting transistor to deliver current at the collector terminal and the terminal capacitance.

3. Transistor dissipation due to transient effect 1 and 2 set an upper limit to the average pulse repetition frequency of the circuit equal to approximately one-fifth the value of the transistor frequency cutoff (\( \alpha_{dc} \)), i.e., the use of 10 megacycles, (mc) \( \alpha_{dc} \) transistor result in a circuit pulse repetition frequency (prf) of about 2 mc maximum.

4. The accumulation of charge on capacitors \( C \) by the transmission of trigger energy through it sets an upper limit to the maximum prf of about 0.15\( \alpha_{dc} \).

5. It is important to note that restrictions number 3 and 4 allude to the average maximum prf; the "burst" repetition rate can be considerably higher. This can be shown as follows:

Let \( g = \text{accumulated charge on capacitor} \ C \) during one trigger pulse

\[
\text{Since } g = C \Delta E
\]

where \( \Delta E \) represents the change in voltage across \( C \) caused by one trigger pulse; then

\[
g \leq iT
\]

where \( T = \text{time between trigger pulses} \) and \( i = \text{charge current necessary to just discharge} \ C \) in time \( T \)

Baker—Symmetrical Transistor Logic
Thus, as $T$ is made small, i.e., the pulse repetition frequency is increased ($1/T = \text{prf}$), then $\Delta E$ increases and at the limiting prf both transistors will be conducting at the same time (which usually causes one of them to burn out). In order to prevent $\Delta E$ from becoming too large, $t$ must be increased (to discharge $C$ in time $T$) by decreasing the values of $R$ and $R_b$. There is a practical limit to increasing $t$, however, because decreasing $R$ increases the transistor drive, thus lengthening the transistor storage time which in turn increases the transistor dissipation. However, this is an average effect and the burst prf (say for an interval of 100 trigger pulses) can be a factor of 3 to 5 higher.

6. It should also be noted that the network of Fig. 3 is triggered at all four points simultaneously, which minimizes the delay time without resorting to speedup capacitors across the coupling resistors $R$, and consequently rendering a flip-flop that is exceedingly difficult to false-trigger through load transients.

D. Logic

General

In most of the low-speed (below 500 kc prf) data processing systems built by the group to date, the nets have been constructed with diodes utilizing trailing-edge logic and pulse-level gating of the voltage mode. (Diodes must be able to sustain the full logic levels voltages in the reverse direction.) Transistor emitter follower circuits have been used internal to the nets, where additional current gain is needed. In higher-speed data processing systems (above 500 kc prf) current mode diode nets are used and delays are inserted to circumvent race problems. (Current mode nets are nets that operate with low voltage swings; the current is shunted from one path to another as in Fig. 4.)

Low-Speed Logic

1. Trailing-edge logic

An example of the trailing-edge logic is shown in Figure 5. Since each flip-flop can deliver 20 milliamperes, (ma) and each gate draws 1 ma, the “fan out” from a flip-flop to single level gates is 20. The “fan in” (number of gates that can drive a flip-flop) is almost unlimited. When 2-level nets are used the fan out is 5.

2. Multilevel nets

When more than two levels of logic are used, emitter followers are employed as shown in Fig. 6. This process “and-or-if-and-or” can be carried on indefinitely with two exceptions. They are: 1. that care is taken to guard against too much negative power being fed from the nets back into the flip-flops and, 2. that the nets do not oscillate. The first condition can be overcome by shunting resistors across the input to the nets (note that this wastes power) or using clamp diodes across the flip-flop outputs. The second condition is prevented by inserting buffer inverters after every fourth level in the nets. The over-all fan out for general two level nets of the voltage mode is 5.

3. Capacitor resistor diode gating (CRD Gating)

A simple inexpensive method of pulse-level gating is shown in Figure 7. CRD gating also has the advantage of built-in delay to circumvent circuit races. The disadvantage to this gating method is that it is inherently slow, the maximum speed (or minimum time between gating operations) being limited to about three times the time-constant $RC$. Another limitation is the signal-to-noise ratio unless care is taken to limit the clock pulse amplitude to less than the gate waveform amplitude. However, this latter limitation is easily taken care of with symmetrical circuits in that the wave-form amplitudes are automatically limited to the supply voltage values.

E. Negative Resistance Circuits (NRC)

General Comments

The fully symmetrical bistable circuit discussed in Section II-C (Figs. 2 and 3) can be used to generate very fast rising and falling transients (sharp leading and falling-edge square waves for example). However, for the reasons discussed, the circuit cannot be operated at a prf that would seem consistent with the fast transients. There are several specific reasons why this is so; but generally one can say that the circuits employ a great deal of “speedup” over drive (via the base-to-base capacitors) and since conventional speedup cannot be obtained without reactive elements, the energy stored during the transient period must be recovered during the circuit “rest” (static) interval.

It happens, however, that circuits can be built with much higher repetition rate with little sacrifice of transient time. This is accomplished by utilizing p-n-p and n-p-n transistors and coupling the two together to form a negative resistance circuit, then paralleling two such negative resistance circuits to form a bistable circuit.

Baker—Symmetrical Transistor Logic
Bistable Negative Resistance Circuit

1. Static conditions
Consider the circuit of Fig. 8. When two transistor of opposite types are connected as shown in Fig. 6(A), the resulting circuit is as if a negative resistance was connected between the emitter terminals. The gain of this network can be easily controlled by external means as indicated by the loop current gain equation shown in the figure; i.e., the current gain $G_L$ is primarily dependent upon the product of the ratios $R_1$ to $R_2$ and $R_a$ to $R_4$ (assuming $a, a_p \approx 1$). Thus, if two such circuits are emitter-coupled as shown in Fig. 6(B), the “on” pair will be stable if $R_1 > R_2$ and $R_a > R_4$. It is also important to note that from the application point of view this circuit is very designable in that $+E$, $-E$, $R_n$, $R_b$, $R_3$ may be varied independently rendering design easy for a variety of power supply values, etc. Also, the stability of the circuit is grounded base current gain sensitivity; i.e., $\alpha$ sensitivity, not $\beta$ sensitivity which the circuit stable for a wide range of transistor parameters.

2. Transient conditions
The fact that the ultra-stable network of Fig. 8(B) may be made unstable is shown in Fig. 9. Referring Fig. 9 when the “off” pair ($T_a$ and $T_b$) is turned on, the emitter resistances ($R_1$ and $R_4$) are shunted by the base resistors ($R_3$ and $R_4$) of the opposite transistor pair ($T_1$ and $T_2$). This is an unstable situation as may be seen from the current gain equation of Figure 8(A). (Note: Under no condition, except when the transistors have a common base current gain less than one-half, can the conducting pairs have a gain less than unity.) Under these conditions the four transistor combinations can be characterized by two parallel negative resistance supplied by a current source whereby one-half “avalanches on” while the other “avalanches off.” Thus we see that: 1. circuit regeneration is accomplished without speedup reactive components (this situation allows the circuit to be retriggered immediately after the transient without waiting for reactive components to recover), and 2. the circuits allow wide tolerance to: a. transistor parameters, b. supply changes, c. resistor values, and d. temperature (note that under static conditions, the circuits are effectively grounded base).

Experimental circuits designed on the NRC principal utilizing graded-base transistors have been operated at pulse repetition frequencies exceeding 30 mc and are conveniently designed to operate at a prf of 10 mc.

NRC Buffer
A buffer inverter is shown in Fig. 10. The same static and transient conditions...
that apply to the flip-flop are applicable in this case.

Fast Logical Nets

1. D-c coupled
   A practical approach to building fast diode direct coupled nets is to keep the currents through the diodes low (thus enabling the diode to switch on and off quickly), keep the voltage swings low (thus minimizing the effects of shunt capacity) and to use high-gain NRC buffers. This approach is shown in Fig. 11. In addition to keeping the power level low, important considerations of this network are:
   1. The logic is buffered after two levels, i.e., and-or-buffer-and-or-etc.
   2. The circuit utility is increased from a system standpoint by having both inverted and non-inverted output available.
   3. The clip levels are easily adjusted by providing a bleeder network at the base of the right hand n-p-n transistor.
   4. The symmetry of the circuitry and the resulting system organization (supplies, etc.) allow an n-p-n para-phase inverter (NPcj) I easily obtainable by inverting the supplies, diode polarity and transistor types.

2. Fast a-c logical nets
   An example of fast a-c nets is shown in Figure 4. As in the d-c nets the power level is kept small. The net clip level is adjustable through varying the emitter potential (bias).
   Other important considerations for this type of pulse net are:
   1. The a-c load per input reflected to the clock source is minimized because the clock source merely turns off the input diode.
   2. The diode reverse breakdown voltage may be low (2 to 3 volts) which gives the diode manufacturer freedom to concentrate upon diode speed.

3. Symmetry concepts allow the use of "opposite polarity" designs.

4. Optimum speed bias conditions may be utilized for the transistor through the freedom to vary the transformer turns-ratio.

   These considerations show why it is possible to construct a-c nets with a propagation time of 10 millimicroseconds, (mμs) (and-or amplifier propagation time).

Extension of NRC Techniques

   It is the author's belief that NRC techniques offer one of the more attractive approaches for both higher speed and simpler, more powerful circuit design. The reasons for this are:
   1. NRC techniques which utilize p-n-p and n-p-n transistors do give rise to high prf circuitry that is convenient to design and use.
   2. It has been shown¹ that the four-terminal p-n-p-n devices are equivalent to a pair of transistors.
   3. Circuitry work with three-terminal p-n-p-n transistors (RCA thyristor's) show that it is possible to construct a bistable circuit utilizing fewer components than do ordinary techniques (see Fig. 12).

III. Features of Basic Circuit Modules

The various circuit features that directly affect system design are discussed in the form of Tables I through IV. The author would like to point out that it is difficult to discuss the relative merits of different circuit approaches as applied to systems with a finite amount of words. The reason of this is that evaluation by necessity rests heavily upon experience and, hence, judgment, which is difficult

Fig. 18. Building block concept

Fig. 19(A). Low-speed shift register stage

Fig. 19(B). High-speed shift register stage
to set down on paper. This is why the data are presented in tabular form. Every effort has been made to make the tables as complete as practically possible; and it is only after long deliberation and even then in some cases with reluctance that the quantitative values have been assigned. The key to the qualitative description is:

Excellent . . . almost all that could be desired
Very good . . . noncritical, performs well
Good . . . all right under almost all conditions with normal care
Fair . . . . . . works, but some care in design must be taken

In special cases where further explanation than that given in the tables is needed, the comments appear in the appendices.

IV. Physical Properties

A. CIRCUIT MODULES

As noted in the introduction, the data processing group represented has chosen to sacrifice economy of components in order to save on “the circuits-to-system” realization time (the desirability of this is discussed further in Section V). Fig. 13 is a typical flip-flop board with associated input and output nets. The computer (which is now a working prototype) was built in about 30 staff years. Original estimates for the time to build this system was about one-hundred staff years. Considering the cost of research and development in a modern research laboratory per staff year, it is difficult to see how any other possible circuit-system techniques could have yielded a lower total prototype system cost. Indeed if one now projects the saving in time (staff years) along with the time advantage of having a working system for research studies (our major goal), we believe one will find a total saving in actual dollars by a factor of 2 to 4 over any other possible approach. If one further projects the saving in time to construct other data processing systems with the powerful time-saving circuit techniques discussed, it is difficult to see any other circuit solution for this work.

V. System Comments

Analysis of the difficulties that were encountered while constructing CG24 showed that some of the fundamental device circuit system problems that are significant are:

1. Use of high-speed transistors. Although this was impossible at the time CG24 was started (early 1956), the use of high-speed devices throughout the machine would lessen the clock source problem by allowing lower power nets to be used as well as utilizing fewer devices.

2. Build the machine into a smaller volume. Surprising though it is, the major trouble with nets arose, not from static considerations but rather from transient considerations. The fan out in problems on a static basis are far less important than propagation time considerations. This is because the solutions to fan out-in problems are simple in nature, where the solutions to propagation time problems are not usually so. Indeed some of the problems involving timing have been found difficult to even analyze, requiring a subtle knowledge of programming, devices, circuits, and hardware techniques.

3. Use of a-c nets. Closely coupled with the just preceding discussion is the practical problem of “debugging” the machine. The more liberal use of a-c nets facilitates the partitioning of nets for trouble shooting without the excessive use of dummy loads, etc.

4. Use of larger modules. The reliability of the machine has been extremely good from the standpoint of component failures. It would seem justifiable then to utilize a higher component packing density and more circuits per board with a resulting saving in space, lead length, etc.

Baker—Symmetrical Transistor Logic

Table I.

<table>
<thead>
<tr>
<th>Circuit Type</th>
<th>Component</th>
<th>Power</th>
<th>Transistor</th>
<th>Noise</th>
<th>Temperature, Degrees C.</th>
<th>Designability</th>
</tr>
</thead>
<tbody>
<tr>
<td>Symmetrical buffer</td>
<td></td>
<td>0.3 μs</td>
<td>-5 mc units</td>
<td></td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>Symmetrical flip-flop</td>
<td></td>
<td>0.05 μs</td>
<td>50 mc units</td>
<td></td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>Trailing-edge gating</td>
<td></td>
<td>0.05 μs</td>
<td>diode delay time</td>
<td>15</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>CRD gating</td>
<td></td>
<td>0.05 μs</td>
<td>diode delay time</td>
<td>15</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Multilevel diode transistor nets</td>
<td></td>
<td>10 μms</td>
<td>5</td>
<td>5</td>
<td>+35</td>
<td>Excellent</td>
</tr>
</tbody>
</table>

Table II. Reliability

<table>
<thead>
<tr>
<th>Circuit Type</th>
<th>Component</th>
<th>Power</th>
<th>Transistor</th>
<th>Noise</th>
<th>Temperature, Degrees C.</th>
<th>Designability</th>
</tr>
</thead>
<tbody>
<tr>
<td>Buffer</td>
<td>Very good</td>
<td>Very good</td>
<td>Very good</td>
<td>Faired</td>
<td>-35 +65</td>
<td>Excellent</td>
</tr>
<tr>
<td>Flip-flop</td>
<td>Very good</td>
<td>Very good</td>
<td>Very good</td>
<td>Faired</td>
<td>-35 +55</td>
<td>Good</td>
</tr>
<tr>
<td>CRD gate</td>
<td>Good</td>
<td>Excellent</td>
<td>Good</td>
<td></td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>Multilevel diode transistor nets</td>
<td>Fair</td>
<td>Fair</td>
<td>Fair</td>
<td>Fair</td>
<td>Good</td>
<td></td>
</tr>
</tbody>
</table>

E. COMPUTER COMMENTS

This computer contains about 20,000 transistors and approximately 150,000 diodes. The computer (which is now a working prototype) was built in about 30 staff years. Original estimates for the time to build this system was about one-hundred staff years. Considering the cost of research and development in a modern research laboratory per staff year, it is difficult to see how any other possible circuit-system techniques could have yielded a lower total prototype system cost. Indeed if one now projects the saving in time (staff years) along with the time advantage of having a working system for research studies (our major goal), we believe one will find a total saving in actual dollars by a factor of 2 to 4 over any other possible approach. If one further projects the saving in time to construct other data processing systems with the powerful time-saving circuit techniques discussed, it is difficult to see any other circuit solution for this work.
Baker—Symmetrical Transistor Logic

5. System packaging. Future trends indicate faster devices, circuits and systems. Present packaging techniques will prove the major stumbling block to the realization of fast systems.

6. One of the most powerful system aids that exist is a flexible set of circuits, particularly in this era of rapid technology advances. With this in mind, the building block concept shown in Fig. 18 is considered to be important. The circuit makes use of a basic NRC flip-flop (T2 through T5) along with a set of delayed outputs (T6 and T7) and a set of input amplifiers (T8 and T9). The circuit may be made more universal by supplying a set of delay switching current sources (T4 and T3) to completely circumvent circuit races.

VI. Universality of Techniques

Fig. 19(A) shows a single-stage diagram of a Low-Speed Shift Register (up to 500 kc prf). Fig. 19(B) gives the circuit diagram for a high-speed shift register (up to 10 mc prf). The principal feature of the low-speed stage is the ability to drive heavy loads. The main feature of the high-speed stage is the fast shift rate that can be attained.

It is believed that these techniques are well suited to: 1. realizing digital-data processing systems from basic circuits in a minimum length of time; 2. advancing the circuit art as such; 3. rendering feedback information to the device field; 4. using the most powerful logical techniques. Therefore, they should prove interesting to and be used by: 1. any industrial concern interested in prototype machine design, large or small; 2. any research and development concern that is primarily system-oriented where the circuits are a means to a system end; 3. any establishment interested in studying the device-circuit-system relationship, i.e., component manufacturers, educational institutions, etc., because it is felt that the circuits represent realistic compromise in the device-circuit-system area for present and future techniques, and because the circuits and associated techniques are based upon fundamental consideration, realistic limitations, and practical experience.

Appendix I. Propagation Time

1. Symmetrical buffer. Fig. 1

The delay time through the circuit is approximately equal to the sum of the conducting transistor (old state) minority carrier storage time, and the rise (or fall) time of the transistor to be turned on. The minority carrier storage in the transistor to be turned off is shortened by the fact that a large current is drawn from its collector by the opposite conducting transistor. The fall (rise) time of the output is fast because standby current is not required and, therefore, all of the collector current of the conducting transistor (new state) is available to charge shunt capacity and to drive the load.

2. Symmetrical flip-flop. Fig. 3

Since the symmetrical flip-flop is formed from two buffer inverters, the propagation time is about the same as that for the buffer inverter circuit, i.e., about 0.3 μs for 5 mc transistors, and about 0.03 μs for 50 mc transistors.

There is no loop delay in the circuit because the initial transient does not require feedback as the circuit is triggered.

Appendix II. Multilevel Net Propagation Time

The propagation time of a multilevel net (type shown in Fig. 4) is difficult to set because the time depends upon the power (impedance) level at which the net is operated. However, nets of this type can be readily built which exhibit a propagation time of about 0.1 μs per stage utilizing ordinary diodes and 5 mc transistors.

References


IBM Current Mode Transistor Logical Circuits

J. L. WALSH
NONMEMBER AIEE

The CURRENT mode circuits discussed in this paper and in preceding papers are intended for use in a very large, high-speed digital computer. From the circuit standpoint, this machine could be classed as a mixed synchronous-asynchronous system in which the outputs of chains of logic are often sampled by clock pulses. The system requires circuits which have delays of approximately 20 millimicroseconds per circuit. The basic circuit philosophy discussed here is well suited to the properties of the drift transistor.

Properties of the Transistor

The speed of response of a transistor switching circuit, neglecting stray capacitances, depends on the frequency response and the time constant of base resistance-collector capacitance. Of equal importance is the delay due to minority carrier storage, particularly when this delay approaches the maximum to which one wishes to restrict a circuit. As an example, if one wishes to restrict the circuit delay to 20 millimicroseconds and the saturation delay is 10 millimicroseconds, then only 10 millimicroseconds can be allowed for the transition to the switching threshold of the stages being driven. However, if the saturation delay is eliminated, a full 20 millimicroseconds can be allowed for transition to the switching threshold of the load stages. Clearly, then, a transistor switch operated out of saturation will not have to produce as steep rise or fall times to maintain the same circuit delay as a switch which is driven into saturation.

The frequency response and the collector capacitance are marked functions of the d-c operating point. The situation for a drift transistor is shown in Fig. 1, where curves of constant frequency cutoff and constant collector capacitance are plotted as a function of collector-to-base voltage and collector current. The collector capacitance varies inversely with the 1/3 power of collector voltage, but remains relatively constant as current is varied over a wide range. The contours of constant frequency cutoff bear some resemblance to a family of rectangular hyperbolas. In general, frequency cutoff increases as collector reverse bias is increased. However, for a fixed value of collector voltage, the frequency cutoff will decrease when the current exceeds the optimum value shown in Fig. 1. Also, the frequency cutoff is poor at very low currents.

The curves of Fig. 1 indicate that when a transistor operates on a load line such as $x$, frequency response and collector capacitance will approach an optimum within the hyperbola of allowable power dissipation. The disadvantage of this load line is that, when on, the transistor is required to dissipate more standby power than would be required with a load line that extended into the saturation region.

Basic Current Mode Switch

Consider the basic current mode switches shown in Fig. 2. The circuits are differential amplifiers with one input reference to ground in the p-n-p circuit, and -6.0 volts in the n-p-n circuit. The input signal to the top transistor, $T_1$, swings about ground, but only by an amount sufficient to switch current completely into either transistor $T_1$ or $T_2$.

In the p-n-p circuit of Fig. 2 the top transistor, $T_1$, is off when the input potential is at +0.4 volts and the bottom transistor, $T_2$ is conducting. When the input potential is at -0.4 volts, the bottom transistor is biased off and the top transistor conducts. Since the potential changes at the input are very small the 910-ohm resistor and the +6-volt supply constitute a constant current source, and there is little difference in the current supplied to the top or bottom transistors. The output signal is developed across the 240-ohm load resistor returned to -6 volts. In order to make the output signal swing about -6.0 volts, a small current bias is added through the 2.45K resistor returned to -12 volts. With this arrangement, the output potential varies from an off value of -6.4 volts to an on value of -5.6 volts.

The p-n-p circuit of Fig. 2 has an input referenced to ground, and outputs referenced to -6 volts. Because of the 6-volt difference between input and output, a p-n-p switch cannot drive another p-n-p...