2) Machine time is used efficiently, since no time need be lost waiting for input-output devices to complete their operation. Other machine activity may proceed meanwhile.

3) Each input-output device may be treated separately for programming purposes. Efficiency of operation is obtained automatically when several separately programmed devices are operated simultaneously, although average- and peak-rate limitations must be considered.

4) Maximum flexibility in programming for input-output devices is obtained. The full power of the central machine may be used by each input-output sequence if desired. Routines for each device may be as long or as short as the particular situation requires.

5) The modular organization of the input-output equipment simplifies additions and modifications to the complement of in-out devices.

6) The organization of buffering storage allows the amount and kind of such storage to be tailored to the needs of the individual devices and the data-handling requirements to be met by the system.

7) The multiple-sequence program technique appears to be particularly well suited to the operation of a large number of relatively slow input-output devices of varying characteristics, as opposed to a smaller number of high-speed devices.

Memory Units in the Lincoln TX-2*

RICHARD L. BEST†

Memory Units in the Lincoln TX-2 Computer

There are 3 high-speed live memories in TX-2; all are random access and all use ferrite cores. The largest is the $6\frac{1}{2}$-µsec cycle time “S” memory with 65,536 37-digit words. The “T” memory is entirely transistor driven; it has a capacity of 4096 37-digit words and a $5\frac{1}{2}$-µsec cycle time. The smallest and fastest is the “X” memory with a capacity of 64 19-digit words; external word selection and 2 cores per bit make possible an access time of 0.8 µsec and a cycle time of 4 µsec.

“S” Memory (65,536 Words)

The “S” memory (Fig. 1) is a coincident-current magnetic core unit with a storage capacity of 65,536 37-bit words. The bits in the word are read out in parallel with a cycle time of 6.5 µsec and an access time of 2.8 µsec. (Cycle time is the time between successive strobe pulses and access time is the minimum delay between setting the address register and strobing.) The block diagram (Fig. 2, opposite) shows that two 256 position magnetic core switches are used to supply the READ and WRITE current pulses to the X and Y selection lines. The operating characteristics of these switches are such that the contents of the address register are no longer needed after the READ half of the cycle, and the interval between READ and WRITE may be extended several microseconds under computer control to permit the other operations to occur. Two coordinates are used to select a register during READ and three coordinates are used for WRITE. In each case, 2:1 current selection ratio is used. The S memory with 604 tubes and 1406 transistors, is a 37-digit version of the 19-digit TX-0 memory that has been described in the literature.¹ The basic operation of this type memory has also been described and will not be repeated here.²

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From the collection of the Computer History Museum (www.computerhistory.org)
Best: Memory Units in the Lincoln TX-2

"T" MEMORY (4096 WORDS)

The 4096 37-bit word memory is also a coincident-current magnetic core unit. The bits of the word are read out in parallel with a cycle time of 5.5 µsec and an access time of 2.4 µsec. A timing diagram is shown in Fig. 3. The computer program can extend by any amount the interval between READ and WRITE. Again, a 2:1 current selection ratio is used with two coordinates used to select for READ and three coordinates for WRITE. A total of 1460 transistors and 64 diodes are used (not counting the address and buffer registers and control).

Mechanical Features

The 64×64×38 (one spare plane) pluggable array (Fig. 4) is contained within a 5-inch cube. The cores used at 47 mils OD, 27 mils ID, and 12 mils thick. The material is similar to General Ceramics’ S-1, and is also used in the S memory.

Selection Circuits

The logic and circuitry of the memory address register decoder is shown in Figs. 5 and 6 (next page). The input to the emitter follower AND gates is a dc level of zero or −3 volts. Silicon diodes add a bias shift without the loss that would be associated with a simple voltage divider. The +1.2 volt supply for the inverter AND gates is a single divider for the whole memory—the load on the divider is constant.

Each inverter AND gate feeds a selection line driver (Fig. 7). Q4 passes the full selection line current (+ and −250 ma) and is selected to have a minimum β of 10 for current of either polarity. The transient back voltage of the selection line for this current is 12 volts. The series connected emitter followers (Q1 and Q2) supply the large amount of current needed to cut off Q3 quickly during selection.

The load for Q2 is such that a large surge of current is delivered to Q3 to turn it on quickly when this line is deselected.
Fig. 6—One channel, emitter follower and inverter AND gates, "T" memory.

Fig. 7—One channel, selection line driver, "T" memory.

Digit Circuits

The input of the digit plane driver shown in Fig. 9 is a standard logic level of 0 or -3 volts. Q2 acts as a switch which connects a voltage source across the digit winding and the parallel RC combination. It can be turned on and off very quickly by virtue of the large overdrive of current into its base which is supplied by the combination of Q1 and its collector load. The adjustable resistor is used to set the correct dc inhibit current which is measured across the 2-ohm resistor, and the 0.001-μF capacitor is used to speed the current rise time in the digit winding.

In the sense amplifier shown in Fig. 10 two 160-ohm resistors terminate the sense winding and tie it down to ground. Constant dc emitter currents are supplied to Q1 and Q2 by the 13k resistors. A stable dc collector-to-base voltage results from the voltage divider comprising the 1.3k resistors which form a virtual center tap on the sense winding operating in conjunction with the 3.3k resistor. Thus, with the dc emitter current and the base-to-collector voltage stabilized, the operating point of Q1 and Q2 is stabilized. Two 60 μF electrolytic capaci-
Q5 but can be interrupted by an input signal large enough to overcome the bias on the 68-ohm resistor. The 5k variable resistance is adjusted so that a 50-mv input signal will be just enough for this purpose. The normal ONE input signal is 100 mv. All of the +10 volt marginal check lines are tied together so that the sense-amplifier clip levels may be remotely checked to determine the memory margins.

"X" MEMORY (64 WORDS)

There are three modes of operation of the "X" memory:

1) READ-WRITE,
2) READ, and
3) CLEAR-WRITE.

The external-word-selection magnetic-core unit using 2 cores per bit has a storage capacity of 64 19-bit words. The bits of the word are read out in parallel with a cycle time of 4 μsec and an access time of 0.6 μsec. In this memory, cycle time is the time between successive strobe pulses with a repetitive READ-WRITE cycle; access time is again the minimum delay between setting the
address register and strobing. A total of 434 transistors, 8 diodes, and 1 vacuum tube are used excluding the address and buffer registers and control.

Operating Principle

The winding configuration of the single plane unit is shown in Fig. 11. A word is selected externally by connecting the upper end of a word line (pt. Y, for instance) to a fixed point. The READ driver then puts out a current pulse \( 4\frac{1}{2} \) times that required to switch a core on a 2:1 basis (Fig. 12). Only one of the two cores (per bit) is switched to the cleared state by this pulse because any previous WRITE operation would have left one core set, and one cleared. The switched core generates a pulse in its digit line. This line passes through one of the cores in the same direction as the word line and through the other core in a direction opposite to the word line. Thus, the polarity of the pulse on the digit line during READ, indicates whether a ONE or a ZERO is being read out.

Current always flows in the digit winding. The polarity is controlled by the flip-flop associated with that digit, and the amplitude is \( \frac{1}{3} \) of the required switch current in a 2:1 system. The digit current is swamped out by the large read current and therefore has no effect during READ. During WRITE, a current of \( \frac{2}{3} \) is sent down the selected word line. The digit current adds to the write current in one core and subtracts from it in the other, so that one core has a current of unity and the other a current of \( \frac{1}{3} \). Thus, the current ratio used during WRITE is 3:1 with a disturb current of no more than \( \frac{1}{3} \). Fig. 12 shows the timing and current relationships in cores A and B of Fig. 11.

The cores used for the “X” memory are 47 mils OD, 27 mils ID, and 12 mils thick. The core material is similar to General Ceramics’ type S-3 which differs from S-1 in that the coercive force required for switching is lower, and the switching time is longer. We needed the low coercive force so that we could drive the cores with transistors.

Access time remained short because, even with transistors, we could overdrive the cores during READ. Each winding makes 4 turns on each core through which it passes. Fig. 13 (opposite) shows the complete memory plane (4\( \frac{1}{4} \times 6\frac{1}{4} \) inches) and Fig. 14 shows a portion of it enlarged. The cores are mounted on a lucite plane; the wires pass through openings made by the intersection of milled slots on one side of the plate with similar slots on the other side milled at right angles to the first. With each winding making 4 turns per core, the digit current is 8 ma, the write-driver output current is 18 ma, and the read driver current is 117 ma.

The block diagram is shown in Fig. 15. The particular method of word selection used is determined partially by the computer’s use of the outputs of the j-bits decoder. Two write drivers are used and the output of the first level selection determines which one is used.

Selection Circuits

One channel of the selection circuit is shown in Fig. 16. The j-bits decoder uses 5-way emitter follower AND gates which drive parallel inverters (Q6 and Q7). The collector load of these transistors is such as to provide an overdrive of base current into Q8 or Q9 during both selection and deselection. When neither read nor write driver is active, the word lines are free to float between 0 and -10 volts. Only one of the first-level selection transistors (Q10 or Q11) will be saturated, so base current flows only into either Q8 or Q9. The read driver generates a negative pulse so that the large read current (117 ma) flows in the normal direction in the 2N123’s.
The write current flows in the reverse direction, but it is only 18 ma, and does not require a very high reverse \( \beta \). It would have been more economical of transistors to use a decoder such as that in the “T” memory, but access time is at a premium here, so that the faster circuit was used.

**Read-Write Drivers**

The read driver shown in Fig. 17 (next page) consists of three SBT transistors in series (because of the voltage needed) driving a 6197 to saturation. The back voltage presented by the cores to this driver is constant because, as mentioned before, it always switches one of the two cores in each pair. The 5:1 transformer holds the tube load to a low value.

The write driver (Fig. 18) is very simple—the current in the 1640-ohm resistor is switched into the memory load during WRITE by saturating Q2 which cuts off Q1. Since the selection circuits are returned to \(-3\) volts, the output terminal of this circuit is always below ground.

**Digit Circuits**

The digit driver (Fig. 19) is connected directly to the corresponding flip-flop in the buffer X register. One of the two transistors is always saturated so that current always flows in the digit winding and in a direction determined by the flip-flop. The terminals of the digit winding are connected to input stage (Q1 and Q2) of the sense amplifier shown in Fig. 20 which responds to the voltage difference between the inputs. The open circuit
READ signal on the digit winding is a \( \frac{1}{2} \mu \text{sec} \) pulse \( \pm \frac{1}{2} \text{volt} \) in amplitude. The sense amplifier loads the winding to reduce the pulse to about half this amplitude. A saturation signal is fed to the gates Q3 and Q5 so that the strobe pulse forces the flip-flop to the correct position. If the signal on the free end of the digit winding is positive the flip-flop is left in the same state; if it is negative the flip-flop is complemented.

**Modes of Operation**

There are three modes of operation of the X memory:

1) READ-WRITE,
2) READ, and
3) CLEAR-WRITE.

READ-WRITE has been described above. The READ operation, used when the contents of two registers are needed quickly, performs the necessary function of clearing both cores in each bit before writing. When the computer returns to WRITE in registers that have had a READ cycle only, the CLEAR-WRITE cycle is used. CLEAR-WRITE is the same as READ-WRITE except that the strobe pulse is eliminated. Actually, a WRITE cycle alone would be sufficient but the CLEAR-WRITE cycle was added as an aid to program trouble shooting, since if a WRITE operation should follow a previous WRITE operation on the same register, some bits would have both cores set. A subsequent READ would clear both cores, their outputs would subtract in the digit winding, and the response of the sense amplifier would be unpredictable.

**Acknowledgment**

The results reported above were due to the efforts of many people associated with core-memory development at Lincoln Laboratory.

Major contributions to the system and circuit design were made by S. Bradspies, G. A. Davidson, D. H. Ellis, and J. L. Mitchell. E. A. Guditz was responsible for most of the ideas incorporated in the mechanical design and packaging.
Discussion

D. J. Theobold (U.S.N.E.L.): What type of core material was used?

Mr. Best: The cores for all our memories are made at M.I.T. so we do not have direct counterparts. Two larger memories use the materials which are quite similar to General Ceramics' S-1. It switches in one microsecond. The core material used in the index memory is a very low-gravity, coarse material that is not square enough to be used in the two-to-one selection. It switches with a driving current of 110 milliamp-turns.

E. E. Jungclas, Jr. (Hughes Aircraft): What are the operational temperature limits?

Mr. Best: The relatively high-speed core is used in the two larger core memories, with a high enough Curie temperature for most land base applications. The index memory that is used has quite a bit of zinc in it, in order to get the cores to force down. The Curie temperature of that is relatively low.

Jan Rajchman (RCA Laboratories): What is the inside diameter of the 0.047-inch cores?

Mr. Best: The inside diameter is 27 mils.

David Zeheb (General Electric): Would you amplify on the manner in which you use two cores per bit in the index memory?

Mr. Best: The two cores used in this particular bit are A and B (Fig. 10). The reason for using two cores is so that during "read" one can overdrive the cores very heavily, and switch them quickly, and therefore get short access time. You can only use two cores per bit when you have external selection, that is, some external active element for each word. The read current only goes through these cores, and it does not disturb any portion in the whole range. The main reason for going into the two cores per bit is to get a short read time. When you have two cores there are actually four possible states of those cores; you can have both clear, or both set, right after you have read you have both cores cleared. But you never have both cores set, at least never on purpose. The primary reason for going into two cores was to get a fast read time (indicating on slide). A current of ½ is set in the word line and a current of ¼ in the digit winding. These two windings are wound so that they add in one core and subtract in another. So, depending upon the polarity of the current in the digit winding, only one of the two cores would be set.

R. L. Compton (Librascope, Inc.): Do you mean to imply that the magnetic core memory system was operative to temperatures of the same order as the Curie temperature of the cores?

Mr. Best: No. The room is air-conditioned.

Transistor Circuitry in the Lincoln TX-2*

KENNETH H. OLSEN†

Circuit Configurations

Only two basic circuits are needed to perform most of the logical operations in the TX-2 computer; a saturated transistor inverter and a saturated emitter follower. To the logical designer who works with them, these circuits can be considered as simple switches which are either open or closed.

The schematic diagram of an emitter follower and the symbol used by the logical designers is shown in Fig. 1.

![Emitter follower schematic](image1)

**Fig. 1**—Emitter follower.

With a negative input, the output is "shorted" to the −3-volt supply as through a switch. When several of these emitter followers are combined in parallel, as in Fig. 2, any one of them will clamp the output to −3 v.

![Parallel emitter follower schematic](image2)

**Fig. 2**—Parallel emitter follower.

We have then an OR circuit for negative signals and an AND circuit for positive signals. The transistor inverter is shown in Fig. 3 (next page) with its logic symbol. Basic AND, OR circuits result from the connection of these simple switches in series or parallel (Figs. 4 and 5). More complex networks like the TX-2 carry circuit use these elements arranged in series-parallel (Fig. 6).

In Fig. 3 the resistor \( R_1 \) is chosen so that under the worst combinations of stated component and power...