Design of a Basic Computer Building Block

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FOREWORD

In the past, circuit design of a basic transistor building block consisted of design by successive approximations, where known operating circuits were improved upon by using laboratory techniques to wire up new circuits and then the working properties of these new circuits were evaluated by measurement. A technique for designing and regulating the characteristics of a new circuit with a minimum of laboratory verification is described. Most of the actual work is accomplished by a large scale digital computer, the Univac Scientific.

The use of the digital computer in these circuit designs makes possible a degree of circuit investigation which was hitherto impractical to perform because of time and manpower limitations in the laboratory. The Univac Scientific can, in a few hours, do years of circuit investigation.

Fig. 1 shows a team developing circuits. One member is a circuit engineer experienced in circuit development. The other member is a mathematician experienced in Univac Scientific operation.

Fig. 1—Operating the Univac Scientific.

GENERAL

In this case, the goal was a type of transistor dc inverter circuit having several "or" inputs and several "and" outputs. The general design is shown in Fig. 2.

The computer proves a most valuable tool for the circuit design, once the circuit equations are established. Not only can the computer determine which circuit best meets the specifications, but it also is able to determine just how acceptable the optimum circuit is.

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Fig. 2—Basic building block circuit.

The design is accomplished in two phases. Phase one consists of developing the circuit equations. The computer is then programmed to solve these equations while commuting the variables for two reasons: first, to find all possible solutions and to indicate all those combinations which are not solutions of the desired circuit, and second, to determine and print the particular solution which best meets the desired circuit specifications.

The input to the computer would be component specifications and desired circuit performance specifications. The computer then searches for the value of resistors that would meet these circuit specifications when all the components are in the worst possible end-of-life conditions.

Phase two consists of a series of equations which indicate if the circuit is operative with the values programmed into these equations. The program varies the circuit parameters about the nominal values for the "best" circuit computed in phase one. Failure points are then established for different values of the circuit parameters. Curves are plotted to show areas of circuit operation and areas of circuit failure.

PHASE I—DEVELOPING THE EQUATIONS

The equation of a circuit may be developed by several methods, one of which employs straightforward classical circuit theory analysis. A spot-check is maintained on the equations by inserting values of circuit parameters in the equations to determine actual operating conditions. Another method is that circuits may be set up and their operation noted, and from these observations, relationships can be observed to derive the equations necessary to express the circuit. A close check must be made in the laboratory to be certain that none of the approximations made in the development of these equations may have a detrimental effect on the final results.
The design equations for the transistor inverter are developed as follows:

The time constant equation for the over-all circuit is:

\[ T = R_L C_W \]  

where

- \( T \) = time for capacitor to charge to 63 per cent of its final value
- \( R_L \) = resistance of circuit in ohms
- \( C_W \) = capacity of circuit wiring.

But, from Ohm's law,

\[ R_L = \frac{E}{I}. \]  

So that substitution of \( R_L \) in \( T \) produces the linear approximation for rise or fall time of the circuit:

\[ T = \frac{E C_W}{I}. \]  

This circuit is to be used in a digital machine and only two states of the circuit have to be considered. These two conditions occur at end-of-life operation and are defined as the most extreme voltage levels which can possibly appear on one output. These signal voltages are thus defined as \( E_0 \) and \( E_2 \), where \( E_0 \) is the signal voltage at the worst case above ground, and \( E_2 \) is the signal voltage at the worst case as determined by \( V_3 \).

Substituting \( E_0 \) and \( E_2 \) in place of \( E \) in (3) and adding the expression \( I \) as the current in the load.

\[ T = (E_0 - E_2) C_W R_L / V_4. \]  

Eq. (4) now gives the first approximation of the speed of the circuit, \( T \) being the rise or fall time of the circuit (the time required to make the circuit switch from one state to another state of signal level).

Next, to determine the amount of power dissipated in the transistor designated as \( T_2 \) in the circuit, the power in this transistor can be defined as the current flowing through the transistor times the voltage across this transistor in the worst case, or:

\[ P = N E I \]  

or

\[ P = - N V_4 Y_4 / R_L. \]  

where

- \( N \) = the number of outputs
- \( V_4 \) = the voltage on the collector electrode
- \( V_1 \) = the voltage tied to the load resistor
- \( R_L \) = the resistance of one load.

The next design equation to be defined is for the value of \( R_5 \). The value of this resistor can be defined as

\[ R_5 = E / I \]  

where \( E \) is the voltage across this resistor in the worst case and \( I \) is the current through this resistor in the worst case, now defining \( E \) as the voltage in the circuit,

\[ E = (E_4 - V_3) \]  

and defining \( I \) as the current necessary to drive the worst case load,

\[ I = (V_1 - E_2) N / R_L B_{T_2} \]  

where \( B_{T_2} \) is the current gain of the transistor designated as \( T_2 \). By substitution of (8) and (9) into (7), a direct relationship to determine \( R_9 \) is found:

\[ R_9 = B_{T_1} (E_2 - V_3) R_L / N (V_1 - E_2). \]  

Next, it is necessary to derive the necessary current input to transistor \( T_1 \) which would be necessary to propagate the signal to the output of \( T_2 \). This current can be defined as \( I_D \). In the worst case, the input current \( I_D \) is equal to

\[ I_D = V_4 / B_{T_1} R_5 \]  

where \( B_{T_1} \) is the current gain of the transistor designated as \( T_1 \).

The next design equation to be defined is for the value and of \( R_5 \). The value of this resistor can be defined as

\[ R_5 = - E_2 Y_3 \]  

where \( E_2 \) is the value of a binary signal. Also:

\[ I_7 = V_1 Y_4. \]  

After substitution of the values for \( I_5 \) and \( I_7 \) from (13) and (15) into (12),

\[ - E_2 Y_3 = V_1 Y_4 + I_D. \]  

It should be noted that (17) has variables of \( E_2 \) and \( I_{co} \), but the amount of drive necessary to excite \( T_1 \) is also of interest. This may be defined as \( I_D \), the current necessary to supply the base with sufficient drive to operate the circuit. Solving for the value of \( R_3 \) and \( R_4 \), which will then satisfy both binary conditions of the circuit for the \( E_3 \) conditions proceeds as follows:

\[ I_5 = I_7 + I_D \]  

and

\[ I_5 = - E_3 Y_3 \]  

where \( E_3 \) is the value of a binary signal. Also:

\[ I_7 = V_1 Y_4. \]  

So substitution of (19) and (20) in (18) gives

\[ - E_3 Y_3 = V_1 Y_4 + I_D. \]
Eqs. (14), (16), (17), and (21) may be solved simultaneously, and it is found that

\[ R_s = E_a - E_b/(I_{co} + I_D) \]  
(22)

and

\[ R_a = V_i/(-E_a V_s + I_{co}). \]  
(23)

We solve for the value of \( R_s \), the resistor which is between the input diodes,

\[ R_s = E_a - V_s/(I_D + I_t). \]  
(24)

Since

\[ I_I = V_i R_4 \]  
(25)

substitution of (25) in (24) yields:

\[ R_s = E_a - V_s/(I_D + V_i/R_4). \]  
(26)

The equations developed from (1) to (26) are those which express the absolute circuit conditions which must be met with no circuit supply voltage variation or no resistor change from designed resistance. As there must be an allowance made for changes in resistance and changes in voltages new variables must be added to the equations. These may be defined as

\[ \Delta = + \text{Resistance tolerance} \]
\[ \delta = + \text{Resistance tolerance} \]
\[ G = + \text{Voltage tolerance} \]
\[ H = + \text{Voltage tolerance}. \]

A series of equations may now be set up which will allow the Univac Scientific to solve and determine what limits may be placed on such parameters as rise and fall time, transistor current gains, values of \( I_{co} \), etc. This series is called the programmed equations.

**Programmed Equations**

**Step 1**

\[ R_s = + N V_i V_s G^2 / P_{st} \]  
(27)

**Step 2**

Pick next smaller RTMA value = \( R_{LT} \)

**Step 3**

\[ P_s = N V_i V_s / R_{LT} \]  
(28)

**Step 4**

\[ P_M = P_s G^2 \]  
(29)

**Step 5**

\[ R_s = R_{LT} B_T \delta / K N \Delta \]  
(30)

**Step 6**

\[ K \text{ starts at 1 and is incremented by 0.1 step in the loop to a maximum of 2} \]

**Step 7**

Pick next smaller RTMA value = \( R_{ST} \)

**Step 8**

\[ I_D = - V_i G / P_{ST} R_{ST} \delta \]  
(31)

**Step 9**

\[ R_s = (E_a \Delta / 3 - E_b / \Delta) / (I_{co} \Delta / 3 + I_D) \]  
(32)

**Step 10**

Pick next smaller RTMA value = \( R_{ST} \)

**Step 11**

\[ R_s = V_i H / (E_s \Delta / 3 R_{ST} + I_{co} \Delta) \]  
(33)

**Step 12**

Pick next smaller RTMA value = \( R_{ST} \)

**Step 13**

\[ R_s = (E_a - V_s \Delta) / (I_{co} \Delta / 3 + V_s H / R_{ST} \delta) \]  
(34)

**Step 14**

Pick next smaller RTMA value = \( R_{ST} \)

**Step 15**

\[ T_s = (E_a - E_b) C_w / (V_i (1 - R_{LT} + 1/R_{ST}) H / \Delta + V_i H / R_{ST} \delta) \]  
(35)

**Step 16**

\[ F_T = (E_a - E_b) C_w / [(V_i H / R_{LT} \delta) - (V_i B_{ST} H / N R_{ST} \Delta)] \]  
(36)

**Step 17**

Check value of (36) against value of (35). If (36) is larger than (35), go back to (30) and increase \( K \) to the next larger value. If (35) is larger than (36), print answer. In any case, do not increase \( K \) past 2.

**Note:** \( T_P \) and \( T_S \), from (35) and (36) were derived by making the linear approximation for rise and fall time while taking into account the effect of loading, where one inverter was driving \( N \) other inverters.

The programmed equations now make possible the computation of many circuits with each having different end-of-life limits, transistor gains, supply voltages, wiring capacity, signal levels, etc. With all the pertinent parameters commuted and different circuits computed, it becomes a simple task to pick the optimum circuit for a given set of specifications. Fig. 3 shows a sample format used as output of the computer to indicate the necessary parameters and quantities to meet specifications.

<table>
<thead>
<tr>
<th>( R_{PS} )</th>
<th>( R_{P_T} )</th>
<th>( P_{S} )</th>
<th>( P_{T} )</th>
<th>( N )</th>
<th>( \Delta )</th>
<th>( \delta )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( P_{ST} )</td>
<td>( I_s )</td>
<td>( R_{LT} )</td>
<td>( R_{ST} )</td>
<td>( R_{ST} )</td>
<td>( R_{ST} )</td>
<td></td>
</tr>
</tbody>
</table>

**Fig. 3—Sample format.**

**Phase II—Checking**

Once a circuit has been chosen which can meet the desired design standards, a new set of equations are developed which are called the checking equations. These checking equations check circuit operation with a change in circuit components. If a resistor changes or if a resistor and voltage input change simultaneously, these checking equations will indicate just how much the circuit elements may change with the circuit still meeting the desired design standards.

The checking equations are as follows:

\[ -(E_a + V_i/R_s R_s V_s + V_s = 0 \text{ or } (\text{fails-}) \]  
(37)

\[ E_a + R_s (V_s/R_s - I_{co}) = 0 \text{ or } (\text{fails-}) \]  
(38)

\[ (E_a - V_s) B_s/R_s - (V_s - E_s) N/R_s = 0 \text{ or } (\text{fails-}) \]  
(39)

\[ R_s - (E_s' - E_s) C_w / (V_s R_s + 1/R_s + V_s R_s) \]  
(40)

\[ F_T + (E_s - E_s') C_w / (-V_s R_s - V_s B_s R_s + N R_g) \]  
(41)

Eq. (37) checks the current in the collector circuit of transistor \( T_1 \) to determine if it is sufficient to maintain the dc level required by the circuit.

Eq. (38) checks the circuit to determine if the leakage current in transistor \( T_1 \) will not degrade the circuit operation.

Eq. (39) checks the current requirements of transistor \( T_1 \) to determine if it has enough current output to drive the required output loads.
Eqs. (40) and (41) check rise time and fall time respectively. These equations determine if variations in circuit parameters will increase the rise or fall time so that circuit specifications are violated.

With these checking equations, it is now possible to find the failure points for the circuit, and these points may be plotted in individual curves. The variation in one component is plotted against variation in another. This curve would now show which circuit elements are most critical. This evaluation now points the way towards a revision of the original equations to obtain a circuit which is even more impervious to component variations.

Fig. 4 shows a component curve developed about one parameter, $R_L$, all others being varied about their nominal value. All positions inside this curve denote circuit operation.

The selection of the RTMA values from a table is carried out in the following way. The calculated resistance value is divided by the next smaller power of ten to bring it into the range of the stored table itself. After locating the next smaller tabular value, it is multiplied by the original power of ten. Fig. 5 (next page) shows an over-all organization of this phase.

For a typical program there are ten values of $P_m$, seven pairs of values of $\Delta$ and $\delta$, four values of $N$, and five pairs of values of $B_T$ and $B_P$. This results in 1400 different circuits to be analyzed. The calculation, which takes 3 hours of computing and output time, is done in floating-point arithmetic for ease of programming.

**Description of the Program for Phase I**

The first part of the program, which is passed through only once in the run, forms the various differences and products that would remain constant throughout the run for the particular circuit under consideration. The “sub-setup” program then combines these results with the parameters to be commuted, i.e., the transistor current gains, the number of inputs, and the resistance tolerances. The “sub-setup” is used wherever one of these parameters is commuted. The initial setup and the sub-setup programs shorten the actual calculation of the programmed equations a great deal. It then remains to run through the equations with various values of $P_m$, maximum power in the emitter-follower transistor.

**Description of the Program for Phase II**

In the list of the circuit parameters, the program considers the first variables as the dependent variable and the second (then the third, then the fourth, etc. successively) as the independent variable, hereafter referred to as $Y$ and $X_i$ respectively. For the nominal value of $Y$ there is a test to see if there is a failure at 150 per cent of the nominal value of $X_i$, and if so, $X_i$ is increased in 5 per cent steps and failure is tested for until it finally occurs. These failure values are recorded and the $X_i$ variable is tested at 50 per cent of nominal value for failure. If it fails again, $X_i$ is decreased to the failure point and the results recorded. Otherwise, if there is no failure no changes are tried. After both sides of $X_i$ have been tested for a given $Y$, the $Y$ value is increased by 5 per cent and is analyzed as before. This is continued until the $Y$ variable either fails on a nominal value of $X_i$, or 150 per cent of the nominal of $Y$ is reached. In either case the same procedure is carried out for decreasing $Y$ by 5 per cent increments until, again, either a failure on nominal value of $X_i$ occurs or 50 per cent of $Y$ is attained.

At this stage the variable $X_i$ and $Y$ can be interchanged and the same analysis carried out. This interchange enables the program to follow the lines of failure completely across the 50–150 per cent interval considered, in most cases, although the calculation and the output time is almost doubled. However, there is surprisingly little duplication done due to this interchange. The variables are again interchanged to their original positions before a new independent variable is selected.

After one pair of variables has been completely analyzed, a new independent variable is taken and again the analysis is carried out. When all possible independent variables have been used for an initial $Y$, a new dependent variable is chosen and the set of computations for that dependent variable is accomplished for the remaining independent variables. See Fig. 6 for the program organization of Phase II.

In the given problem there are 15 variables and therefore 105 distinct pairs to consider. The calculation time is about one minute per pair of the average including output time. One may then expect the problem to run almost two hours before completion.
CONCLUSION

The method of design discussed here determines a way to utilize the Univac Scientific to do the detail work in developing circuits. It necessitates a minimum of engineering time to fully explore the circuit possibilities. As detailed an analysis which may be obtained with the Univac Scientific would either take years of laboratory work to obtain, or would not even be considered. Not only is the computer used to optimize the circuit, but it is also used to determine how well this optimum circuit will operate.

Discussion

Mr. Alman: The best circuit here is selected after the computer has calculated as many of the circuits as the designer feels might be of value; and the circuit designer then looks to the tabulated forms, plots the characteristics of these circuits, and picks the circuit which he feels has the widest power for components, and will best meet the circuit requirements.

Gunther Machol (IBM): How much time is required to produce the solution you have shown?

Mr. Alman: Six or seven hours to design the circuit, and about the same time for checking it. Of course, the minute you start doing this sort of thing you realize how many more circuits you might like to look into, and how much you might expand. We had one system set up which would take us something like three months to compute, so you can get into this pretty deeply. I would like to add at this time that this work was all done on the UNIVAC Scientific.

John Paivinen (General Electric): Why does not the transistor cut-off frequency appear in the rise-time relations?

Mr. Alman: The analysis we have shown has been simplified as much as possible. We have expanded the equation to take this fact into account. The drive current is known as is the reaction of the transistor to this current; this just adds an extra time to the rise-and-fall equation.

T. P. Holboran (National Cash Register, Dayton): How long did formulation program, trouble-shooting program take?

Mr. Alman: We had three people working on this development, and it took in the neighborhood of about three months to develop one circuit. Once we had the program going well, we could put a new circuit together in about a week, put it through the computer, and get results.