A Medium-Speed Magnetic Core Memory

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INTRODUCTION

The steady evolution of the state of the art in coincident current magnetic core memories leads constantly in the direction of an all-transistor system of appreciable proportions. Several organizations have been at work in this field, but the system herein described is the first of its type. It is presented to demonstrate one of several possibilities in achieving an all-transistor memory of 150,000 bits.

The engineering design and the construction of the memory for the Transac S-1000 Computer was contracted to Remington Rand UNIVAC. The computer itself is designed and constructed by the Philco Corporation. The memory requirements are for a 36-bit parallel system with 4096 words of storage with special provisions for reading and restoring specified thirds of any word. Rigorous limitations on weight, volume, and power input were imposed which together constituted an extension in the state of the art when the effort was originally started. Some of the circuit designs will undoubtedly seem awkward in view of the improved transistors now available; however, as computer units, they represented the state of the transistor art and market.

GENERAL DESCRIPTION

The logical block diagram shown in Fig. 1 (next page) is introduced here to present a general idea of the entire system. The system is a conventional one using coincident current and inhibit digit control to operate on all 36 bits of the data word in parallel.

The information furnished to the memory by the computer consists of the 12-bit memory address, an initiate signal, the type of operation to be performed (either read, write, or partial write), and the data word or partial data word which is to be written. These signals enter the memory circuitry through buffer amplifiers which convert the computer signals to signals which are compatible with memory circuitry.

Address information is translated in two parts, that which operates the X-coordinate lines and that which operates the Y-coordinate lines. The results of the translation controls drive line switches (current diverters) which provide the coincident current selection of the addressed word.

The initiate signal sets the lock-out flip-flop of the memory timing chain which causes the generation of the first timing pulse. Further stimulation of the timing system is not necessary as additional timing pulses are self-generated. Timing pulses are furnished to appropriate points to govern the sequence of events throughout the memory cycle. The timing of the memory operation does not vary whether a word is being read from memory or a word is being written into memory. The difference between these two operations lies in the control of the gates at the inputs of the memory data register (memory input/output register). To read the memory, the read probe gates \( (RT_n) \) are energized; to write into the memory, the write probe \( (WT_n) \) gates are energized. These gates are controlled by the \( (WRITE)_n \) flip-flops, which store information regarding the type of operation to be performed.

The digit plane control contains all the circuitry necessary to operate 1-bit plane. This includes the sense amplifier, the memory data register and its input gates, and the inhibit/disturb current generator. One-word information transmissions to and from memory are made through the memory data register.

Information furnished to the computer by the memory consists of the word read from memory, a transfer-complete signal which indicates the word is available in the memory data register, and a reference-complete signal which indicates the memory cycle is finished.

MEMORY CONSTRUCTION

The memory cores are assembled in 38 printed circuit frames, each of which contains 4096 magnetic memory cores. The cores are arranged in a 64 × 64 configuration (see Fig. 2), p. 59. Two of the core memory frames are reserved as spares.

The magnetic cores are General Ceramics Type S-3 ferrite material which requires a magnetizing force of approximately 350 ma-turns. This type core was selected for its compatibility with transistor current carrying capacity, power dissipation, and voltage and current gain characteristics. Prior to assembly in a core plane, all the cores are individually tested and selected for uniform characteristics. During the test, the cores are subjected to 320 ma full-amplitude current pulses and 190 ma half-amplitude current pulses. When tested with these current pulses, only those cores which met the following specifications were selected for use in the memory: (See Fig. 3)

1) Disturbed "1" output—14 to 18 mv after being subjected to a series of half-amplitude read current pulses.
2) Disturbed "0" output—7 mv maximum after being subjected to a series of half-amplitude write current pulses.
3) Switching time—4.5 ± 0.5 μsec.
4) Peaking time—2.2 ± 0.25 μsec.

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Fig. 1—Logical diagram, magnetic-core storage.
Fig. 2—Magnetic-core matrix.

Fig. 3—Memory-core output signals.

The waveforms of the "0" and "1" signals induced on the sense wire are shown in Fig. 3.

Four wires pass through each core: an X-coordinate drive line, a Y-coordinate drive line, an inhibit/disturb drive line, and a sense wire, as shown in Fig. 4.

The sense wire of each core memory plane passes through each core once and is wired diagonally in a symmetrical balanced arrangement so that nearly all unwanted noise signals of all cores except the core being addressed tend to cancel.

The inhibit wire passes through all cores in each core memory plane parallel to one of the coordinate drive lines so that when an inhibit pulse (of opposite polarity to the write pulse) occurs, the magnetic field established on this coordinate line is cancelled.

The memory is mechanically divided into two sections because of space limitations. Each section consists of 19 core memory planes and 2 printed circuit terminal boards. The front terminal board of one section is used to buss together all the drive lines of each coordinate. Single wires from the busses are connected to the outputs of the X and Y read/write current generators. The rear terminal boards are used to connect the two sec-
tions, and the front terminal board of the second section connects each drive line to the collector of individual current-diverting transistors.

It has been determined that the magnetic coercive force varies with temperature to such a degree that operation with fixed drive currents over the full range of ambient temperature would not be reliable. To overcome this, the memory is contained in a thermally insulated box and the temperature within the box is maintained constant, slightly above the highest ambient.

**MEMORY TIMING**

A study of the sequence of timed events which occur during a memory reference, revealed the fact that the requirements for timed pulses and their duration remains fixed regardless of the type of operation and the repetition rate of memory references. This permits the use of a timing device which is not synchronized with computer timing. Therefore, the timing of the memory can be separate from the computer timing, and requires only the receipt of an initiate pulse from the computer. A resume pulse must be supplied to the computer when the reference is completed. This principle is used in the timing system which employs magnetic switch cores to create accurately shaped pulses and transistor switches to set and read the cores. Fig. 6 shows the timing circuit used in the memory.

Transistor Q1 is biased to cutoff, and a current $i_1$ flows in the primary winding of the magnetic switch core of sufficient magnitude to hold the applied magnetic field of the core at $+B_s$ (point $A$) on the hysteresis loop. When transistor Q1 is turned on by the positive going input pulse, a saturation current, $i_2$, flows which reverses the applied magnetic field of the core. When this occurs, the magnetic field rapidly traverses the hysteresis loop to $-B_s$ (point $B$) and sets the core in approximately 1 μsec. A negative going pulse is produced at the output. This pulse is not used. At the termination of the input pulse, transistor Q1 again cuts off, and read current $i_4$ begins to flow, producing a positive going pulse in the secondary. This voltage is clamped by diode $CR_1$. The waveforms shown in Fig. 6 illustrate the voltage relations of the transistor and magnetic core.

The output of the first stage is connected to the input of a second stage so that during the interval that the first core is being read out the second stage transistor is turned on thereby setting its associated core. The subsequent operation of the second stage is like that of the first stage, but it is displaced by one pulse period. Similarly, many stages could be connected in series producing as many pulses (time displaced from each other) as is desired.

The emitter resistor, $R_e$, serves the useful purpose of providing the high input impedance ($\text{Beta} \times R_e$) necessary to cause the clamping diode to conduct, without seriously reducing reverse base current. In this manner, the response of the transistor (rise and fall time) is made sufficiently fast so that there is no time lost between pulses of adjacent stages.

The pulse width produced by this method of clamping the output of a magnetic switch core can be accurately controlled so that the pulses produced by many stages are very nearly constant in width. Assuming that magnetic saturation is reached during switching, the core outputs will differ only by that amount of variation caused by differences in saturation flux and by differences in the forward drop of diode $CR_1$. By precise manufacture and selection of cores, and the use of high conductance diodes with very low forward drop, the variation in pulse width between stages has, in actual circuits, been limited to $\pm 0.05$ μsec. The magnetic switch core used in this application is the Remington Rand Type C core.

It was found that a pulse chain of 10 stages, each producing 2-microsecond pulses, best suited the memory timing requirements. Fig. 7 shows the various pulses required, and Fig. 8 is the simplified block diagram of

![Fig. 6](https://www.computerhistory.org)
the memory timing chain. A 1-\(\mu\)sec initiate pulse sets the lockout flip-flop which in turn causes the simultaneous readout of the first stage of the chain. To accomplish this, the first stage transistor is normally conducting so that its associated core is normally in the "set" state. The flip-flop output cuts off the transistor and the core is readout. The lockout flip-flop is reset by a resume pulse taken from a stage near the end of the chain so that a reference cannot be initiated while one is already in progress. Read, write, and inhibit pulses which initiate the respective current driver circuits are generated in proper pulse width by connecting the set and reset inputs of flip-flops to the appropriate timing pulses. Timed pulses are used directly to clear the memory data register and to generate the probe pulses and the post write disturb pulse. It should be noted that the pulses preceding the probe pulse and the pulse which sets the inhibit flip-flop are variable in width. This is accomplished by making the voltage \(E\), across the secondary winding of the magnetic core, variable. This allows for a manual adjustment of the probe pulse timing and beginning of the inhibit pulse so that they occur at the proper time.

A decided disadvantage of the system is its inherent voltage sensitivity. That is, a change in any one of the three negative voltages, \(-20\), \(-18\), or \(-22\) volts, will cause either a malfunction of transistor \(Q_1\) due to insufficient base current, or, a change in pulse width due to a change in voltage \(E\) (shown in Fig. 6). These defects have been overcome by deriving all negative voltages from the same source which is regulated to \(\pm 1\) per cent. In addition, a Zener diode voltage reference for the voltage \(E\) may be utilized.

**Logical Decision Elements**

The logical circuitry employed to operate the memory consists of simple diode AND and OR circuits. The logical AND circuit is shown in Fig. 9. In this circuit, the presence of a logical "1" is defined as ground

![Fig. 7—Memory timed pulses.](image)

![Fig. 8—Simplified block diagram of memory timing chain.](image)
potential at an input. When any of the three inputs \((A, B, C)\) are grounded, the voltage at the output will be 0 volts. When all three inputs are open circuited, and only in this condition, the voltage at the output will be \(-2\) volts (clamped by diode \(CR_1\)). Thus, the latter state defines the logical AND function.

The logical OR circuit (Fig. 10) operates in a similar manner, but diodes \(CR_1, CR_2,\) and \(CR_3\) isolate input circuits from each other so that the presence of a logical “1” at any one of the inputs is capable of causing the output to change to \(-2\) volts.

The output of these buffing and gating circuits is connected to a resistive divider network \((R_4\) and \(R_4\) of Fig. 11) which controls the bias on an SB100 transistor. When the voltage at point \(I\) is zero, a small reverse bias is applied to the transistor, holding it in the cutoff state. When the voltage at point \(I\) falls to \(-2\) volts, base current is supplied to the transistor and it conducts. Signal inversion in the transistor complements the output of the AND and OR circuits as shown by the accompanying Boolean expression. The output diodes in the collector circuit connect to logical circuits similar to the input circuitry of this stage. These diodes serve to isolate the different logical circuits connected to the same transistor.
In order to provide the direct uncomplemented output, it is necessary to connect the output of a single inverter amplifier to a second inverter amplifier. In this case the first stage is used to drive two second stages so as to provide additional outputs.

By connecting the collector of one single inverter to the OR input of a second single inverter, and vice versa, a bistable flip-flop can be constructed as shown in Fig. 12. Outputs from the flip-flop can be taken directly via diodes from the collectors to connect to other logical circuitry.

The three basic circuits: the single inverter, the double inverter, and the flip-flop, provide all the logical control throughout the memory. This includes memory address translation, read and write probe, temporary data storage, and inhibit/disturb logic.

The read or write probe logical signals gate the proper transmission paths connecting to the inputs of the memory data register. The read probe pulse energizes the gates connected to the sense amplifier so that the memory word enters the memory data register. The write probe pulse energizes the gates in the lines from the computer X register so that a new word can enter the memory data register. The memory data register controls the inhibit/disturb gates, thus causing the contents of the memory data register to enter the memory.

There are three different write probe signals; \( WT_1 \), \( WT_2 \), \( WT_3 \) and three different read probe signals \( RT_1 \), \( RT_2 \), and \( RT_3 \). Each of these signals controls the read and write gates of 12 bits of MDR. The \( RT_1 \) and \( WT_1 \) signals control bits 0–11; \( RT_2 \) and \( WT_2 \) signals control bits 12–23; and \( RT_3 \) and \( WT_3 \) signals control bits 24–35. This method of gating permits the reading of the whole word from the memory, writing a whole new word into the memory, or writing new information into a specified sector of the memory.

The read and write probe signals are produced through the use of the logical circuits shown in Fig. 1. Inverse logic is employed to create the read probe signals. One of the four flip-flops shown may be set by a signal from the computer at the same time that a memory reference is initiated. Flip-flop \( W_0 \) is set if an entire new word is to be written in the memory. Flip-flop \( W_1 \) is set if new information is to be written in bits 0–11; flip-flop \( W_2 \) is set for bits 12–23, and flip-flop \( W_3 \) is set for bits 24–35. The flip-flops are cleared at the end of the reference by a pulse from the timing chain. The proper outputs of the \( W_0 \) flip-flop are combined with the proper outputs of the \( W_1, W_2, \) and/or \( W_3 \) flip-flop outputs into the correct logical gates. The results of these combinations are combined with the probe pulse from the timing chain.

Therefore, if none of the flip-flops are set, all three of the read probe signals will be present allowing the whole word from the memory to enter the memory data register. If the \( W_0 \) flip-flop is set, all three of the write probe signals will be present allowing the whole computer word to enter the memory data register. If the \( W_1 \)
The flip-flop is set, the $WT_1$, $RT_2$, and $RT_3$ pulses will be present, allowing bits 0–11 of the $X$ register and bits 12–35 of the memory to enter the memory data register, etc. The other read and write functions are formed similarly. Subsequently, the contents of the memory data register are written into the memory.

The manner in which the memory data register controls the inhibit/disturb generators, which, in turn, controls the writing of "1's" or "0's" into the memory, is shown in Fig. 13. The memory data register is cleared by a 2-μsec pulse at the beginning of the memory reference in preparation for receipt of the new word from memory, or the $X$ register, or a combination of both. The output of the sense amplifier and the read probe gate is shown connected to an OR circuit with the output from the $X$ register and the write probe gate. The "1" output of the memory data register is connected to the $X$ register while the "0" output side is connected to an AND gate with the 7-μsec inhibit pulse from the inhibit flip-flops. The output of this gate is connected to an OR circuit with the 2-μsec post write disturb pulse from the timing chain. This line controls the operation of the inhibit/disturb generator. Thus, for those bits in MDR containing "1's," a 2-μsec post write disturb current pulse will appear on the appropriate inhibit/disturb lines, and a "1" will be written into memory. For those bits containing "0's," however, a 9-μsec inhibit current pulse will appear on the appropriate inhibit/disturb lines and a "0" will be written into memory. For the proper timing of these two pulses refer to Fig. 7, current waveforms.

Address Translation and Line Selection

The $64 \times 64$ memory core configuration requires $64$ $X$-coordinate drive lines, and $64$ $Y$-coordinate drive lines. All the $X$-drive lines are bussed together at one end and connected to the secondary of the read/write transformer. The other end of each line is connected to the collector of a bilateral transistor which is turned on by the address translator when selected. The $Y$-coordinate drive lines are connected in the same manner.

Twenty-four buffer amplifier stages are used to make the signals from address transmission lines from the computer (Philco circuitry) compatible with the memory logical circuitry. These are simple isolation transistors in series with the signal lines. The remainder of the address translation (Fig. 14) is quite conventional with the exception that inverse logic is employed to reduce the number of standard logical circuits employed. The address buffers feed 16 three-input "OR" circuits to operate the appropriate double inverter amplifiers for the $X$ line selection. (The $Y$ line selection is made by an identical system.) The outputs of the double inverter amplifiers are fed to 64 two-input "OR" circuits completing the translation. This is followed by single inverter amplifiers which complement the input to restore the proper sense.

The output of the single inverter is connected to the inverter amplifier (A) and then to the line selecting current diverter (D). Fig. 15 is the circuit of the last three stages of the translator. The primary purpose of this circuit is to change the current level from that of the surface barrier transistor to that of the current diverter (200 ma). Transistor $Q_1$ supplies approximately 1 ma to the base of transistor $Q_3$ keeping it in the saturated conductive state. A voltage of approximately $-2$ volts.
Valenty: A Medium-Speed Magnetic Core Memory

Fig. 15—Current diverter schematic diagram.

Fig. 16—Current generator waveforms.

Fig. 17—(a) Inhibit/disturb current generator schematic diagram, (b) transistor Q1 collector characteristics, (c) inhibit/disturb current generator voltage waveforms.

Fig. 17 represents the circuit employed as the inhibit/disturb current generator. The low-frequency transistor (Q3) is biased by base voltage, E1, to conduct at the desired inhibit current magnitude. The high-frequency response transistor, Q4 (Type GT845), is normally cut off and therefore the dc current flowing in transistor Q1 passes into the resistance R3. The transistor Q4 load line (exaggerated) is shown as line A on the graph of Fig. 17. When transistor Q4 is switched into saturation by the proper timed pulse, the collector voltage of transistor Q4 drops rapidly below +8 volts so that diode CR1 is cut off. Consequently all the pre-established dc current

appears at the collector of transistor Q2 and also at the base of transistor Q0. The diverter transistor of only one drive line conducts while all other lines remain cut off. Therefore, the voltage impressed on the collectors of all cutoff transistors will reach the peak voltage produced by the current generators. It is necessary to reverse bias the cutoff transistors at a voltage greater than the expected collector voltage variations. Thus, in this system, Q3 is cut off with 10 volts reverse bias.

When a drive line is selected, transistor Q1 and Q2 cut off, and a 15-ma base current is supplied to transistor Q0. Transistor Q0 is designed with equal forward and reverse gains so that it can easily pass bipolar pulses of equal magnitudes. The response time of transistor Q0 in this circuit is such that a 200-μsec pulse can flow 2 μsec after the base current begins to flow and will cut off 2 μsec after base current ceases to flow.

Constant-Current Generators

The current waveforms required to operate the memory are shown in Fig. 16. The inhibit/disturb current generator produces either of the two pulses shown. The inhibit pulse is a 9-μsec pulse which overlaps the write current pulse and is of opposite polarity to it. The occurrence of this pulse causes a 0 to be written into the addressed memory core. The disturb pulse is a 2-μsec pulse occurring immediately after the write pulse whenever a 1 is written into the addressed core. This places the core in the disturbed 1 state immediately so that the half-disturb noise signal is greatly reduced during subsequent memory references involving either of the two coordinate drive lines which pass through this core. This results in greater uniformity of 1-signal output from all cores.

Several factors were taken into account in the design of the constant-current generators; regulation of current magnitude for variation in load or supply voltage, stability of current magnitude regardless of transistor gain, ease of varying current magnitude, and the transient response of the power supply.

Fig. 17 represents the circuit employed as the inhibit/disturb current generator. The low-frequency transistor (Q3) is biased by base voltage, E1, to conduct at the desired inhibit current magnitude. The high-frequency response transistor, Q4 (Type GT845), is normally cut off and therefore the dc current flowing in transistor Q1 passes into the resistance R3. The transistor Q4 load line (exaggerated) is shown as line A on the graph of Fig. 17. When transistor Q4 is switched into saturation by the proper timed pulse, the collector voltage of transistor Q4 drops rapidly below +8 volts so that diode CR1 is cut off. Consequently all the pre-established dc current
of transistor Q1 now flows through the inhibit/disturb line in the form of a current pulse. Load line B is representative of the condition during the flat portion of the current waveform.

During the transition period, the collector capacity charge variation tends to increase the collector current which causes an overshoot followed by a drooping waveform due to the slow response of transistor Q2. The inductance, $L_1$, is inserted in the emitter circuit to provide degenerative feedback and overcome this undesirable effect. This keeps the collector current constant during the transition periods.

Diode $CR_2$ in series with the inhibit/disturb drive line and the resistor $R_3$ connected to +16 volts serve to reduce the capacitive loading of the read/write current pulses due to the large capacity between the inhibit/disturb drive lines and the read/write drive lines.

Since the memory word length is 36 bits, there are 36 inhibit/disturb generators. It is desirable to be able to manually adjust the current magnitude of all 36 generators by a single control. To accomplish this, despite wide variations in transistor gain, the emitter resistor is used to provide dc stabilization of the circuit. Actually this resistance is made up of the controlled winding resistance of the inductor, $L_1$. Controlling the current magnitude produced by all 36 drivers is easily accomplished by varying the base bias voltage of transistor Q1. Fluctuations in current demand from the power supplies due to the pulsing of the inhibit drivers has been eliminated by maintaining a dc current in the generators, thereby simplifying the design of the +16 volt power supply while permitting the +8 volt supply to vary as much as 10 per cent. This is particularly important since the transient current demand would be quite large (6 to 8 amps) making voltage regulation of low voltage-high current supplies extremely difficult.

The X and Y read/write current generators produce bipolar half-magnitude current pulses which are coupled to the X and Y coordinate drive busses. The current waveforms have a 1-μsec rise and fall time and a 5-μsec flat portion of approximately 175 ma. The circuitry for the read/write current generator is basically the same as for the inhibit/disturb generator except that two generators and a dual primary transformer are required to produce bipolar current pulses.

One of the special considerations that had to be taken into account in the design of the read/write generator was the response of the read/write transformer. Under certain operating conditions, the load as seen by the transformer may not change for long periods of time. This drive line impedance is relatively low and extends the recovery time of the transformer to a period greater than the interval between current pulses. Because of this, the base reference line of the current pulses would tend to seek different levels in either the plus or minus direction depending upon the interval between memory
references and also the degree and direction of unbalance between the read and write pulses. To insure a zero base line at the start of each reference, all of the energy stored in the transformer must be dissipated prior to the next reference. To accomplish this, a secondary line switch was placed in the transformer current return path (Fig. 18, preceding page). The circuit of this switch is the same as the current diverter except that it is normally in the conducting state. At the end of each reference, the switch transistor is cut off for 2 μsec. This presents a fairly high impedance to the transformer secondary winding, and the stored energy dissipates very quickly so that the transformer will be ready for the next reference at the end of each cycle.

**SENSE AMPLIFIER**

The sense amplifier used in each digit plane control is shown in Fig. 19. A 1:1 balanced transformer, $T_1$, couples the memory core output signal into the grounded base input stage $Q_1$. The bias voltages applied cause approximately a 1-ma dc current to flow through the transistor into the auto transformer $T_2$. The 14 to 18 mv signals are amplified to approximately 0.5 volt based at +0.2 v and clamped by the bases of transistors $Q_2$ and $Q_3$. The bipolar pulses are rectified and amplified to the 2 volt level shown. These signals are transmitted to a single inverter to place them in the proper polarity for logical combination with the read strobe signal. The output of transistor $Q_4$ is a 2-volt signal 2 μsec wide, occurring during the read signal. Waveforms at the various points are shown.

The +0.2 volt reverse bias on transistor $Q_2$ and $Q_3$ is sufficient to eliminate all unwanted noise signals which occur at probe time. The wanted signal is sufficient to cause these two transistors to saturate.

**CONCLUSION**

The results achieved in this design clearly indicate that larger and faster all-transistor memory systems are feasible. The power required to operate this memory is approximately 300 w and the space required is approximately 5 cubic feet. This represents a power reduction over an all-tube equivalent of about 10 times and a weight and volume reduction of about 20 times. The performance of the 1200 transistors used in this system has yet to be demonstrated but it is felt that it will be far better than the vacuum-tube equivalent.

**Discussion**

**S. C. Chao** (General Electric): What is the accuracy of the driving currents?

**Dr. Valenty**: Plus or minus 50 milliamperes, or approximately 10 per cent.

**E. Slobodzinski** (I.B.M.): What is the environment temperature-wise that your system was designed to operate in? What have you considered as the worst case for component and transistor tolerances?

**Dr. Valenty**: The system is designed to operate up to 90 degrees F; over that it is automatically turned off.

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