A HIGH-SPEED MULTICHANNEL ANALOG-DIGITAL CONVERTER

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Introduction

The large-scale tests of aircraft, missiles, and components necessitate the recording of many parameters. These parameters are usually converted by transducers or pick-up devices to voltages proportional to the magnitude of the physical quantity being measured. The many resulting voltages may be recorded for later analysis, used immediately for performance calculations and for control, or they may be both recorded and used immediately. If the data is recorded, it is ideally done on a multi-channel recorder. The quantity of data taken on large-scale tests and the complexity of performance calculations make it desirable to obtain the data in a form suitable for digital computation. Since the final form of the data is frequently digital in nature whether it is recorded for future use or is used immediately for computation, a multi-channel high-speed analog-to-digital converter would greatly simplify the preparation of analog data for digital computation and tabulation. A high-speed multi-channel analog-to-digital converter and a complete data system of which it is a part will be discussed in this paper.

Description of the System

The system was designed for the specific needs of static structural load tests of airframes. The requirements of this system are, however, similar to those of other large-scale tests, differing only in the method of display and in the storage medium. Figure 1 is a block diagram of the entire data system. The inputs are 400 strain gages which must be read and recorded in less than two seconds. Since each strain gage can be in either tension or compression, it is necessary that the system be capable of measuring both positive and negative voltages. The strain gages are energized by a DC voltage giving a DC output in the low millivolt range. Since the system will measure these low voltages, it will work equally well for thermocouples, resistance thermometers, and other pickup devices producing a DC voltage and is not limited in the type of input. The 400 strain gages are sampled in sequence by the commutator which programs the entire recording operation. The actual switching of the inputs is done by 400 sets of mercury relays operating as the plate loads of 400 6L6 tubes. These relays were chosen for their low noise level, long service life, and fast operating characteristics. The relays selected are single-pole double-throw break-before make relays with a closing time of approximately .5 milliseconds. The drop-out time, however, is considerably longer and is not constant. The contacts in the relay consist of two sets of two contacts and a wiper. When the relay is not energized, the wiper connects one set of contacts; where energized it connects the other set. To compensate for the variable drop-out time of the relays, the input signal is connected through the normally closed contacts of a relay to the normally open contacts of the preceding relay. Thus, the closing of a relay connects a gage to the converter and opens the connection of the previous gage, giving a constant period for each channel.
The converter, shown within the dotted lines, consists of a modulator and amplifier, the logical gates and summing networks, the write gates, and, in this system, a clock pulse shaper. The clock pulse is recorded on the magnetic drum and provides the basic frequency for the entire data system. The output of the converter is recorded on the magnetic drum for later recovery through the readout gates and output registers. This system will, in less than two seconds, convert and record the readings of 400 strain gages used in structural tests.

The tests for which this system was designed consist of taking a set of readings on 400 strain gages for each of 20 structural loads. To prevent creep or fatigue at the higher load levels, it is necessary to take the data rapidly and release the load immediately. After each load, the strain is plotted against per cent of full load. Thus, any non-linearity indicating that the elastic limit has been reached is found before structural damage occurs in the member under test.

**Performance of the System**

**Programming**

The programming of the recording system is shown in block diagram in Figure 2. For a recording cycle there are six binary counters and two selector switches required. The logical levels used throughout the converter system are a +20 for true and zero or ground for false. The clock pulse is a 120 KC negative pulse of .1 microsecond duration and a 20 volt amplitude, biased to +20 volts during the off period. The clock pulse originates from the magnetic drum turning 3600 r.p.m. In addition to this clock pulse, there is a single pulse on a separate drum channel for orientation on the drum and four quadrant pulses; the first coincident with the single pulse and a clock pulse, and three others separated by at least 508 clock pulses and coincident with a clock pulse. The negative clock pulse, applied to the grid of the conducting tube in a flip-flop, triggers it to the other stable state. In the block diagram, a square block designates a coincidence or a one to one correspondence between quantities; a circle designates an inverter where a false input results in a true output and vice versa; a triangle with the inputs extending within the triangle designates a sum gate where the output is true if any input is true; and a triangle with the inputs terminating at the side opposite the output designates a product gate and is true only if all the inputs are true.

The "C" and the "D" counters are five stage binary counters gated to count to 24 and 20 respectively and returning to zero with a quadrant pulse. Counter "C" returns to zero also with a 24 count and a clock pulse. K and L are 20 position selector switches which set five double-pole double-throw relays each to a binary representation of numbers between one and 20. When K is advanced one position to the next number, L advances to become the old value of K. The configuration of D, K and L are compared in two coincidence gates and the true signals from each gate are fed to a sum gate; the output of this gate being true whenever there is a coincidence between D and K or D and L. The output of the D and K coincidence gate is also fed to a product gate along with the 24 count of C counter, and the three count (fourth quadrant) of the Q counter. The output of this product gate, which is false
at all times except at the 24 count of C counter when there is a coincidence of D and K in the fourth drum quadrant, is fed through an inverter to a product gate with the clock pulse. The output of this product gate, \( R_x \), is fed along with the output of the D and K or D and L sum gate, to a product gate. The output of this product gate is a string of pulses, coincident with and similar to the clock pulse. In the first three quadrants of the drum this string of pulses will be 50 pulses long; 25 pulses during the coincidence of D and L, and 25 during the coincidence of D and K. In the fourth quadrant of the drum, however, there will be only 49 pulses; 25 during the coincidence of D and L and 24 during the coincidence of D and K. These pulses are counted by the R counter which counts zero to 24 and returns to zero. This counter originally is set at zero, and the zero count regresses 1 clock pulse each revolution of the drum. The zero count is used as the output of this counter and serves to program the entire recording cycle. It is fed to two product gates; one a product with the coincidence of D and K, the other a product with the coincidence of D and L. The product with D and L produces a pulse \( P \) which is used to initiate one conversion cycle in the converter. The second product, occurring 25 clock pulses later, is used to select the next input from the 16 x 25 matrix driven by counters Q, S, and G, and to record the value of the input just converted. Thus, during one revolution of the drum, four inputs are selected and recorded. A particular input is selected and 475 clock pulses later, conversion of its voltage to a digital output is started and 500 clock pulses later it is recorded. With each revolution of the drum, the information is stored displaced one clock pulse later in each quadrant because of the retrograding of the R counter. There are 36 write amplifiers on the drum, and 100 channels are recorded on nine drum tracks each 25 revolutions of the drum. The product gates shown are used for the write amplifier selection.

Since, during a test, it is necessary to examine the results of previous structural loads, the read gates are also shown. In the read programming, a four position \( M \) and a 25 \( N \) switch are added. A coincidence between the \( M \) switch and the Q counter selects the quadrant and a coincidence between the \( M \) switch and the C counter and a coincidence between the D counter and S counter selects the clock pulse address within the quadrant. For oscilloscope display, all readings (20) of a particular input channel are read in 20 revolutions of the drum or in \( \frac{1}{3} \) of a second. For printing the results, one reading is taken each 25 revolutions of the drum or every \( \frac{25}{60} \) of a second. There are only nine read amplifiers which are connected by a selector switch to one of the four groups of tracks formed by the write program. Thus, the input channels are divided into four groups 1-100, 101-200, 201-300, and 301-400 for reading depending on the connection of the read amplifiers. This completely programs the data system used for structural testing of airframes. Not shown on the diagram however, is the 16 x 25 matrix for input selection and the write gates for the write amplifiers.

Converter

The analog-to-digital converter is shown in Figure 3 by block diagrams. It consists of a pulse source, a modulator, an amplifier and filter, a phase discriminator, the summing network, and the logical circuits. The 120 KC pulse generator is driven by the clock pulse channel on the magnetic drum. The clock pulse is used for synchronizing a 480 KC oscillator and for the
logical gates. The 480 KC oscillator is used for the bridge modulator excitation as shown. Two arms of the bridge are matched diodes, the other two arms are resistances. A balance potentiometer is connected as shown for compensation of any initial unbalance. Across the bridge there are a one ohm precision summing resistor, an input resistor, and an output transformer. The output of the modulator, a 480 KC sine wave equal in amplitude to the unbalance voltage across the modulator and of a phase determined by the sign of the unbalance voltage, is amplified and filtered for the input to the phase discriminator. The action of the phase detector will be explained in more detail in Figure 4, but it forms a Z signal which is true for one phase of the modulator output and false for the other. The true Z output indicates a positive voltage across the modulator and the false Z output indicates a negative voltage. This Z signal is used in the logical gates to determine the action of the converting cycle.

A conversion from an analog input to a digital output is accomplished in 16 time intervals defined by the four stage, B counter. The B counter rests in the one state until it receives a pulse P from the programming circuits. It then advances with each clock pulse through 15 configurations and returns to one until the pulse P. The configurations of the B counter are used, with the clock pulse, to trigger the nine A flip-flops. The final state of these nine flip-flops is recorded as the output of the conversion. Nine cathode followers are driven by these nine flip-flops. In the cathode circuit of each cathode follower there is a precision summing resistor clamped by a diode to a reference voltage and connected to the one ohm precision resistor in the modulator circuit. When each cathode follower is conducting, it adds current through the one ohm resistor and generates a voltage across the one ohm resistor. The current, voltage generated, and the digital value of each of the nine cathode followers is shown in Table I along with the time interval in which conducton is started.

<table>
<thead>
<tr>
<th>Flip-Flop No.</th>
<th>Milliamps</th>
<th>Millivolt</th>
<th>Series Resistance</th>
<th>Digital Value</th>
<th>Time Interval</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Thru lr</td>
<td>Across 1 ohm Resistor</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A₁</td>
<td>3.00</td>
<td>3.00 m.v.</td>
<td>5K</td>
<td>100</td>
<td>2</td>
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<tr>
<td>A₂</td>
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<td>1.50 m.v.</td>
<td>10K</td>
<td>50</td>
<td>5</td>
</tr>
<tr>
<td>A₃</td>
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<td>0.60</td>
<td>25K</td>
<td>20</td>
<td>7</td>
</tr>
<tr>
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<td>0.30</td>
<td>50K</td>
<td>10</td>
<td>9</td>
</tr>
<tr>
<td>A₅</td>
<td>0.30</td>
<td>0.30</td>
<td>50K</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>A₆</td>
<td>0.15</td>
<td>0.15</td>
<td>100K</td>
<td>5</td>
<td>11</td>
</tr>
<tr>
<td>A₇</td>
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<td>0.06</td>
<td>250K</td>
<td>2</td>
<td>12</td>
</tr>
<tr>
<td>A₈</td>
<td>0.03</td>
<td>0.03</td>
<td>500K</td>
<td>1</td>
<td>13</td>
</tr>
<tr>
<td>A₉</td>
<td>0.03</td>
<td>0.03</td>
<td>500K</td>
<td>1</td>
<td>14</td>
</tr>
</tbody>
</table>

TABLE I
Through the one ohm resistor there is also a current of 3 mA. from a precision negative supply generating a -3 mV. signal across it. A product of the two time interval and a clock pulse triggers the A1 flip-flop true, causing a current of 3 mA. to flow through the one ohm resistor, generating a +3 mV. signal. This current continues until the 5 time interval when a comparison with the input voltage is made. If Z is true, the product of the clock, time 5, and Z triggers A1 false, if Z is false, A1 is left in the true state and the current continues to flow through the one ohm resistor. The sum of the A1 current and the -3 mA. from the negative supply is zero and thus, the A1 flip-flop determines the sign of the input voltage, remaining on if the input is positive and turning off if the input is negative. A2, which along with A3 through 9, was triggered false at time 2, is triggered true at time 5. The cathode follower for the A2 true generates a current of 1.50 mA. in the one ohm resistor, representing a count of 50. At the 7 time, A2 is left true if Z is false or is triggered false if Z is true. Also, at the 7 time, A3 is triggered true. It results in a current of .6 mA. in the 1 ohm resistor and represents a count of 20. At the 9 time, A3 is triggered false if Z is true and left true if Z is false. Similarly, A4 is triggered true at time 9 and represents a count of 10 (.3 mA.); A5 at time 10 representing a count of 10 (.3 mA.); A6 at time 11 representing a count of 5 (.15 mA.); A7 at time 12 representing a count of 2 (.06 mA.); A8 at time 13 representing a count of 1 (.03 mA.); and, at time 14, A9 is triggered true representing a count of 1 (.03 mA.). In each case, the flip-flop is triggered false if Z is true and remains true if Z is false. At the 16th time interval, if Z were false at time 5, A1 and the 16 time interval cause A2 through 9 to compliment. This is necessary since a -3 mV. is used as a reference and it is desirable to measure all voltages from ground. In this manner, a digital output proportional to the input voltage is generated in 16 time intervals. Since the clock frequency is 120 KC, the total time required for a conversion is 132 microseconds. The code 50, 20, 10, 5, 2, 1, 1 was chosen in this application because it simplified the read-out for display purposes. However, any code can be used by changing the values of the summing resistors. Also, the full scale output can be changed by changing the value of the 1 ohm resistor within the limit that the resistor must be small compared to the other resistors.

Phase Detection

The action of the modulator and phase detector will be made more clear by examining Figure 4. In this figure, the wave forms at the detectors are shown for three input voltages. The lower wave form is the clock pulse, a 120 KC, -20 volt, .1 microsecond pulse. Above it is the delayed clock pulse which is a +20 volt, .25 microsecond pulse delayed 5.67 microseconds after the clock pulse. The lower sine wave shows the wave form from the modulator after amplification and filtering for an input voltage of -1.39 mV. During the first and second time interval, a sine wave proportional to the input voltage is generated. It will be noted that the delayed clock pulse occurs at a negative peak of the sine wave. At the end of the 2 time, the +100 count is added to the one ohm resistor when A1 is triggered true. The addition of the A1 count causes a phase reversal and causes Z to become true when the delayed clock pulse and the positive peak coincide. Thus, at time 5, A1 is triggered false and A2 is triggered true, adding 1.5 mV. to the -3 mV.
across the one ohm resistor. The resultant -1.50 mV. across the one ohm resistor is less than the -1.39 mV. input and again we get a phase reversal. At the 7 time, A2 is left on since the delayed clock pulse is coincident with the negative peak and Z is false. Also at the 7 time, A3 is turned on, adding an additional .60 mV. or a count of 20 to the one ohm resistor. The resultant 2.10 mV. again causes a phase change and causes Z to be true, turning A3 off at time 9. At time 9, .30 mV. or a count of 10 is added by A4 to the 1.50 from A2. The resultant 1.80 is again too great and A4 is turned off and A5 is turned on at time 10. A5 likewise adds .30 mV. or a count of 10 to the 1.50, and is turned off at time 11. At time 11, A6 adds .15 mV. or a count of 5 to the 1.50. The 1.65 mV. is again larger than the input voltage and A6 is turned off at time 12. At time 12, A7 is turned on, adding .06 mV. to the 1.50. Since the delayed clock pulse does not coincide with a positive peak, A7 is left on at time 13 and A8 is added. A8 adds .03 mV. to the 1.56 and remains on at time 14. At time 14, A9 adds a 1 count to the 1.59 mV. and is turned off at time 15. Then since A1 is true, A2 through A9 are complimented at time 16. The resultant output is a count of 20 + 10 + 5 + 1 = 46 or, since each unit represents .03 mV., represents an input of 46 x .03 = -1.38 mV.

The sine wave in the center represents the waveform at the phase detector with a zero input. At time 2, as before, a count of 100 is added and at time 5 is left on since the delayed clock pulse does not coincide with a positive peak. At all other times, the flip-flop is turned false since the sum of A1 and any other flip-flop is greater than zero. At time 16, the number does not compliment since A1 is true and the resultant output count is zero.

In the upper curve, the sine wave represents an input of +1.39 mV. to the converter. Again, at time 2, a count of +100 is added to the -3 mV. reference and is left on at time 5. At time 5, a count of 50 or 1.50 mV. is added and is too great. Thus, at time 7, the 50 count is removed and a +20 count is added. This remains on at time 8 and a count of 10 is added. This remains on at time 9 and another count of 10 is added. At time 11, this 10 count also remains on and a count of 5 is added. This too remains on and, at time 12, a count of 2 is added. This is too large and is turned off at time 13 when a count of 1 is added. This count of one remains at time 14 when another count of 1 is added. This last count is too great and is removed at time 15, leaving an output count of 46 or +1.38 mV.

The phase detector is basically a coincidence circuit between the 480 KC sine wave and the delayed clock pulse. The 480 KC sine wave is clipped and shaped and, with the delayed clock pulse, is fed to the input grids of a 6AS6 gate tube. The output of the coincidence on the 6AS6 triggers the Z flip-flop true and each clock pulse triggers Z false. Thus, Z is false unless triggered true by the phase detector.

Conclusions

This converter has proven quite reliable. The code can be changed quite easily to fit any computer code and the number of significant digits can be increased by utilizing the time intervals not in use. When these circuits were designed, it was felt that these time intervals might be needed to allow
transients to die out but this is not the case. Thus, using this same code, the number of significant digits, with a correspondingly higher input voltage, could be increased to 999 by adding a 100, 200, 500 and 1000 count. Also, the rate of conversion can be doubled by redesigning the gating circuits if more rapid conversions are necessary. Preliminary experiments have indicated that a clock frequency of 1/2 m.c. would not be too difficult to achieve if circuit techniques reducing distributive capacity were used.

Acknowledgments

The author is deeply indebted to Mr. A. Unrauer and Mr. L. Fisher for much of the circuit design and checkout of the circuits described here. Also, he is indebted to the International Research Corporation of Santa Monica for their cooperation in designing and building the magnetic drum and associated circuitry.

Fig. 1. Block diagram - converter system
Fig. 2. Block diagram - programming

TO 16x25 MATRIX FOR CHANNEL SELECTION
Fig. 3. Block diagram - converter
Fig. 4. Waveforms at phase detector

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