MULTI-CHANNEL ANALOG-DIGITAL
CONVERSION SYSTEM FOR D-C VOLTAGES

W. S. Shockency
Hughes Research and Development Laboratories
Hughes Aircraft Company

This report is intended to cover a successive approximation type analog­
digital converter which was designed for use in an airborne digital computer
developed by Hughes Aircraft Company on an Air Force Contract. The unit which
was developed was required to digitalize as many as 32 input voltages and de­
rive the analog voltage from 32 digital output quantities in approximately
15 milliseconds. Critical requirements on space and weight of equipment,
coupled with the large number of inputs and outputs, dictated the use of a
common converter which could be multiplexed on a time basis among the various
inputs and outputs.

Some of the more important specifications to be met were the following:

1. Inputs - 32; 0-100 volts dc; accuracy ± 1/2% of full scale; sampling
time, 200 μsec; sampling rate, 60 cycles; impedance of inputs, 200K
min during sampling time.

2. Outputs - 32; 0-100 volts dc; accuracy ± 1/2% of full scale; sampling
time, 200 μsec; sampling rate, 60 cycles; maximum ramp, full scale
in 1/2 sec; load to be driven, 50K ohm min.

3. Digit rate - 160 kc.

4. The conversion needed to be done so that results were proportional
to a system reference voltage.

5. The equipment was to be production designed to meet JAN specifica­
tions for airborne electronic equipment.

6. Critical limitations on size, weight, and power were to be considered.

7. Reliability requirements of a tactical military system had to be
borne in mind.

Equipment designed to meet these specifications has been built and tested. A
block diagram is shown in Figure 1. It consists of a decoder and inverter
amplifier, which are used in common on all conversions, plus a control unit,
a memory, individual power output stages, and electronic switches for connect­
ing the desired input or output channel into the decoder.

The decoder consists of an 8-digit register, a binary current weighter,
and a comparator amplifier. An analog input is converted to binary code by
a series of comparisons of the input voltage to standard voltages supplied by
the current weighter. The comparator amplifier, through the control unit,
sets up the register according to the results of these comparisons. The
binary-coded input is then shifted by the control unit into the computer
memory for use as needed.
A binary-coded output is converted by shifting it from the computer memory to the register. Each flip-flop in the register controls a gate in the current-weighter which releases a current into the summing point proportional to the significance of the flip-flop. The output of the weighter, through the comparator amplifier, controls the charging of the output memory capacitor. This capacitor is necessary to act as analog memory between sampling intervals.

Figure 2 graphically illustrates the analog-to-digital conversion of an input quantity.

1. Assume that an input d-c voltage of $\frac{7}{8} F_{RS}$ has just been selected by the control unit for conversion.

2. At $T_0$, which is the beginning of the 200-μsec sampling interval, the appropriate input selector switch is closed by control unit signals and the same unit shifts zeros into the register to clear it.

3. From $T_0$ until $T_{100}$, the circuit is permitted to stabilize so that the voltage at the output of the inverter amplifier is proportional to the selected input within ±0.1%.

4. During the interval $T_{100}$ to $T_{200}$, the following staircase sampling takes place, which involves the control unit, register, current weighter, and comparator amplifier:
   a. From $T_{100}$ until $T_{120}$, the half-scale stage of the current weighter is energized by the appropriate register stage and this current is compared with the current from the input; $I$ is proportional to $\frac{7}{8} F_{FS}$. Since the current from the register is not of sufficient magnitude to bring the summing node of the comparator amplifier to the ground reference, this stage of the weighter is permitted to remain "on" by the controlling output signals from the comparator amplifier.
   b. From $T_{120}$ until $T_{140}$, the quarter-scale stage is closed in the weighter and the sum of this current and the half-scale current is compared in a similar fashion, this stage also being permitted to remain on at the end of the sampling interval.
   c. In a similar manner, the control unit closes eighth-scale and the comparator amplifier permits it to remain on; however, from $T_{150}$ until $T_{200}$, as the control unit applies the remaining weighted currents, the comparator amplifier finds that its input has reversed, indicating that the current from the weighter is too great, so the comparator amplifier output signals return the remaining register stages and weighter to the zero state.
d. Consequently, at the conclusion of the sampling interval, the register is set as a binary representation of the input voltage. Since it is an 8-digit register, resolution is 1/256.

e. During the interval $T_{200}$ until $T_{300}$, the register shifts the coded information into the memory and starts the conversion process on the next input voltage.

Since the decoder is fundamentally an output device, digital-to-analog, it could easily be used to derive an output d-c voltage by means of an operational summing amplifier. Such an amplifier would be required to deliver up to 100 volts into 50K-ohm load with a linearity of $\pm 0.1\%$. This was impractical with the limited supply voltages imposed by the use of subminiature tubes. To hurdle this problem, it was necessary to supply a feedback connection from the individual outputs to the input of the inverter amplifier. Because the decoder is time-shared by all the inputs and outputs, electronic switches are used to make this connection. With the incorporation of this feedback, the comparator needed to have only the requisite zero stability, about 10mv, and sensitivity, about 5mv; linearity was of little importance. The use of feedback on this circuit makes possible the use of an on-off type of servo. The power gates consist of two electronic switches, each of which connects a current source to the memory capacitor, one (+) and one (-). These switches are selected by the control unit and operated by the comparator amplifier output. A (-) output connects a (+) source to the capacitor and a (+) output connects a (-) source.

As indicated above, for an output conversion the computed result from the memory is shifted into the current-weighter register and the feedback switch for the associated output is closed. This is done in the first 100 $\mu$sec of the 200-$\mu$sec sampling interval (see Figure 3). The output from the binary weighter is permitted to stabilize during this interval, and the appropriate feedback selectro switch is closed, thereby applying the previously stored analog output voltage to the inverter amplifier for comparison with the new value from the current weighter. From $T_{100}$ until $T_{200}$, the corresponding output power gate receives the proper signal from the comparator amplifier to raise or lower the voltage on the capacitor. If during this interval equilibrium is reached, alternate charging and discharging of the output condenser will result until the control unit disconnects the power gate at the end of the 200-$\mu$sec interval, $T_{200}$.

The loop which is involved in servoing of an output voltage consists of the power gate and the inverting and comparator amplifiers. The sensitivity of this loop, which is essentially the forward gain of the comparator amplifier, and the loop lags are the factors which determine the peak excursions in the servoing of an output voltage for any ramp driving function. It was not difficult to increase the forward gain of the loop so that it was no longer a determining factor and only the loop lags remained. For this design the lags amounted to about 2 $\mu$sec. For the specified ramps this results in hunting of $\pm 1/2$ digit.

The limiting accuracy of this system is mainly determined by the resistors used in the current weighter. To maintain a weighter with an accuracy of $\pm 0.3\%$, it was necessary to use resistors with a tolerance of
+ 0.1%. It was also necessary to control the shunt capacity of the units. As it turned out, this did not impose a problem because many commercially available wire-wound resistors would easily meet our requirement. Wire-wound units were used because there was no other available resistor with the necessary initial tolerance or temperature coefficient.

The zero stability of the system is limited by the electronic switches. To minimize the variation in this offset, dual diodes were paired in such a manner as to take advantage of the closer balance established by JAN controls for diodes in the same envelope. The JAN control imposed gives a spread of ± 250 mv. It may be of some interest that tests of a few hundred diodes from several lots indicated that this spread amounted to only ± 100 mv.

The linearity of these switches was better than ± 0.1%, operated in the circuit over the full range of input-output voltages. Zero stability within the inverting and comparator amplifiers was achieved by the use of chopper-stabilized amplifiers.

Parasitic or undesired capacities and leakage currents were effectively reduced by boot-strapping wherever possible. For example, heater-cathode leakage in the capacitor power gates was troublesome, but it was essentially eliminated by boot-strapping of the filament which was associated with the cathode tied to the memory capacitor.

Final checks on the system proved that the deviations from analog input voltage to binary code and from binary output to analog output voltage were within the basic tolerance of ± 0.5% of full scale. More meaningful information of statistical significance is presently being gathered by using the associated computer in special checking routines. It is hoped that the distribution of error for any possible number may be obtained by this method, which will take into consideration systematic errors due to component tolerance and errors due to all sorts of noise components, such as short- and long-term random component changes.

The size and weight requirements were met by using miniature and sub-miniature components and using advanced packaging techniques, such as etched circuitry. The final weight of the equipment was about 60 pounds and it occupied approximately 1.6 cubic feet. The power consumed by the units amounted to about 650 watts. The figures do not include the drum memory unit.
Fig. 1. Block diagram

Fig. 2. Analog-digital input conversion

Fig. 3. Digital-analog conversion-output