Abstract—In this article, a tutorial on the techniques and procedures used in a production test environment is presented. This overview is structured in such a way that the less experienced test engineer can learn about the common and various methods used in mixed-signal test. Various aspects related to test and their role in the manufacturing process of ICs are discussed. In fact, the paper starts off by motivating the need for testing and then describes the different methods: DC, AC, and dynamic testing as well as clocks, SerDes and RF testing. Design for Test (DFT) techniques are also described.

Index Terms— Mixed-Signal, Analog, DFT, SerDes, RF, Production Test

I. INTRODUCTION

It is well known that testing is an important and essential phase in the manufacturing process of integrated circuits. In fact, the only way that manufacturers can deliver high-quality chips in reasonable times is through an extensive testing process. As outlined in Figure 1 the IC manufacturing process involves three major steps: fabrication, testing and packaging. Nowadays, the manufacturing cost of mixed-signal ICs is being dominated by test. Consequently, testing has become a major factor in profit margins [1]. The three major roles of test engineering are: lowering the costs, reducing the time to market and ensuring excellent product quality. Automated test equipment (ATE), such as that depicted in Figure 2, has long provided a successful test solution for large volume manufacturing. They are highly automated, fast, accurate and traceable. They can be seen as one big closed system of electronics and sensors. In the testing industry, DSP techniques have proved to be very efficient. In fact, DSP based testing reduces test time and allows advanced signal manipulation (e.g., separation of signal components and interpolation between samples to obtain better time resolution). Consequently, most ATE machines are built such that DSP testing is supported.

In this paper, the concepts of measurement accuracy, yield and test time are presented next. Then in Section III, common test methodologies: DC, AC and dynamic testing, are explained through carefully chosen examples. Analog channels and sampled-data channels testing are outlined in Section IV through a voltage follower and an analog-to-digital converter test example. Then, clocks and SERDES devices are discussed in Section V. RF testing concepts are outlined in Section VI. In Section VII, the importance of the test interface and the transmission of signals between the tester and the device under test (DUT) are investigated. Design for test (DFT) techniques are presented in Section VIII along with various embedded test instruments. Finally, conclusions are drawn in Section IX.

Figure 1: IC manufacturing process: fabrication, testing and packaging.

Figure 2: Mixed-signal ATE.
II. YIELD, MEASUREMENT ACCURACY AND TEST TIME

The primary goal of a semi-conductor manufacturer is to produce large quantities of ICs for sale to various electronic markets, i.e., cell phones, ipods, HDTVs, etc. Semi-conductor factories are highly automated, containing IC machines that are capable of producing millions of ICs over a 24 hour period, every day of the week. For the most part, these ICs are quite similar in behavior, although some will be quite different from one another. A well defined means to observe the behavior of a set of large elements such as ICs is to categorize their individual behavior across a range of values and to simply count the number of times a behavior is observed to fall within a particular category. One often normalizes the count by the total number of items in the set, say N, and we can express the fraction in each category as a percentage, or more commonly as a probability. Organizing the data in this manner is known as a histogram and an example is illustrated in Figure 3. Here the offset voltage associated with a device has been identified and collected for each and every IC from the lot and organized into a histogram. We see that 15% of devices produced in this lot had an offset voltage between -0.129 V and -0.128 V. We can conjecture that the probability of another lot produces devices with an offset voltage in this same range is 15%. Of course, how confident we are with our conjecture is the basis of all things statistical; we need to capture more data to support our claim. This we will address in a moment; for now, let us consider the “goodness” of what we produced.

In this section, we consider the “goodness” of a device as defined by the component data sheet. As a data sheet forms the basis of any contract between a supplier and a buyer, we avoid any subjective argument of why one measure is better or worse than another; it is simply a matter of data sheet definition. Generally, the goodness of an analog and mixed-signal device is defined by a range of acceptability as shown in Figure 4, as bounded by a lower specification limit (LSL) and an upper specification limit (USL). These limits would be found on the device data sheet. Any device whose behavior falls outside this range would be considered as a bad device. This particular example considers a device with a two-sided limit. Similarly, the same argument applies equally to a one-sided limit (just a different diagram is used).

A. Yield

Testing is the process of separating good devices from the bad ones and is illustrated in Figure 5. Yield is a measure of the manufacturing efficiency and is given by the expression

\[
Yield = \frac{\# \text{ Good Devices}}{\# \text{ Good Devices} + \# \text{ Bad Devices}}
\]  

The lower the yield the more waste that is produced, and consequently, less profit. As testing is not a perfect process, mistakes are made, largely on account of the measurement limitations of the tester, noise picked up at the test interface and by noise produced by the DUT itself. The most critical error that can be made is one where a bad device is declared as good, as this has a direct impact on the operations of a buyer. This error is known as an escape. As a general rule, the impact that an escape has on a manufacturing process goes up exponentially as it moves from one assembly level to another [2]. Hence, the cost of an escape can be many orders of magnitude greater than the cost of a single part. Manufacturers make use of test metric to gauge the goodness of the component screening process. One measure is defect level (DL) and it is defined as

\[
DL = \frac{\# \text{ Bad Devices Declared Good}}{\text{Total Devices Tested}}
\]

or, when written in terms of escapes, we write

\[
DL = \frac{\# \text{ Escapes}}{\text{Total Devices Tested}}
\]
It is important to note that a measure of defect level is a theoretical concept based on a probability argument and one that has no empirical basis. The argument goes as if we knew which devices were escapes, then we would be able to identify them as bad and remove them from the set of good devices. Clearly, this is a non-causal operation.

Figure 5: Test process showing how good devices are separated from bad ones, but how some bad ones (escapes) get through the screening process.

B. Measurement Accuracy

The cause of escapes in a mixed-signal environment is largely one that is related to the measurement process itself. A value presented to the instrument by the DUT will be corrupted by circuit related errors associated with the instruments; for example, offsets and noise. Let us denote the value produced by the DUT as $V_{DUT}$. Furthermore, let us model the voltmeter as that shown in Figure 6: a DC voltage source representing the offset is placed in series with a noise source and an ideal voltmeter. By KVL, we can write the voltmeter value as

$$V_{MEASURED} = V_{DUT} + V_{OFF} + V_{noise}$$  \(4\)

If we repeat a sequence of measurements involving the same DUT, we would obtain a set of values that would in general be all different on account of the noise that is present. To eliminate the effects of this noise, one could instead take the average value of a large number of samples as the measurement. For instance, if we average each side of eqn. (4) using the short-hand notation $<>$ for the averaging operation, we get

$$\langle V_{MEASURED} \rangle = \langle V_{DUT} + V_{OFF} + V_{noise} \rangle$$  \(5\)

Recognizing that averaging distributes across addition [3], we can write

$$\langle V_{MEASURED} \rangle = \langle V_{DUT} \rangle + \langle V_{OFF} \rangle + \langle V_{noise} \rangle$$  \(6\)

Assuming that the noise process is normal with zero mean, together with the fact that $V_{DUT}$ and $V_{OFF}$ are constants, we find that the average measured value becomes

$$\langle V_{MEASURED} \rangle = V_{DUT} + V_{OFF}$$  \(7\)

As long as the sample set is large, then averaging will eliminate the effects of noise. However, if the sample size is small, a situation that we often find ourselves in practice, then our measured value will vary from one sample set to another. See for example the illustration in Figure 7(a) involving two sets of samples. Here we see the mean values $\mu_{M,1}$ and $\mu_{M,2}$ are different. If we increase the total number of samples collected to say $N$, we would find the mean values of the two distributions approach one another in a statistical sense. In fact, the mean of the means will converge to $V_{DUT} + V_{OFF}$ with a standard deviation of $\sigma_M / \sqrt{N}$ as illustrated by the dashed distribution (orange) shown in Figure 7(b).

Metrology (the science of measurement) is interested in quantifying the level of uncertainty present in a measurement. Three terms from metrology are used in test to describe this uncertainty: repeatability, bias and accuracy. Assume that $N$ samples are taken during some measurement process and that these samples are assigned to vector $x[n]$. The mean value of the measurement is defined as

$$\mu_M = \frac{1}{N} \sum_{n=1}^{N} x[n]$$  \(8\)

The repeatability (also known as precision) of a measurement refers to the standard deviation associated with the measurement set, i.e.,

$$\sigma_M = \sqrt{\frac{1}{N} \sum_{n=1}^{N} (x[n] - \mu_M)^2}$$  \(9\)

For the example shown in Figure 7(b), repeatability refers to the spread of the measurements samples about the sample mean value $\mu_M$. The larger the spread, the less repeatable the measurement will be.
Bias error or systematic error is the difference between the DUT value and the average of a large number of measured values. Bias error can be mathematically described as

$$\beta = V_{DUT} - V_{MEASURED}$$  \hspace{1cm} (10)$$

where $V_{MEASURED}$ is derived through a separate measurement process involving a large number of samples, i.e.,

$$V_{MEASURED} = \mu_M \bigg|_{N \text{ large}}$$  \hspace{1cm} (11)$$

In essence, $V_{MEASURED}$ converges to $V_{DUT} + V_{OFF}$ (the noiseless value) and $\beta$ equals the negative of the instrument offset.

Finally, this brings us to the term accuracy. It is probably the most critical parameter that a test engineer will consider during a production test. As test time is of critical importance during a production test, the role of the test engineer is to make a measurement with just the right amount of uncertainty, no more, no less.

Accuracy is defined as the difference between the DUT value and an estimate of the measured value ($\hat{V}_{MEASURED}$) derived from a measurement process involving a small number of samples. We can expressed this in mathematical terms as

$$\text{Accuracy} = V_{DUT} - \hat{V}_{MEASURED}$$  \hspace{1cm} (12)$$

As an estimate of the value of the measured value, we make use of a probabilistic argument from the theory of estimation. For a set of measurement values consisting of N samples having a mean value $\mu_M$ and standard deviation $\sigma_M$, the probability that the noiseless measured value lies within a range bounded by $\pm\alpha \frac{\sigma_M}{\sqrt{N}}$ of the mean value is given in terms of $\alpha$ as

$$P\left(\mu_M - \alpha \frac{\sigma_M}{\sqrt{N}} \leq V_{MEASURED} \leq \mu_M + \alpha \frac{\sigma_M}{\sqrt{N}}\right) = \begin{cases} 0.667, & \alpha = 1 \\ 0.950, & \alpha = 2 \\ 0.997, & \alpha = 3 \end{cases}$$  \hspace{1cm} (13)$$

One can refer to the $\alpha$ term as a confidence parameter, as the larger its value, the greater our confidence (probability) that the noiseless measured value lies within the range defined by

$$\mu_M - \alpha \frac{\sigma_M}{\sqrt{N}} \leq V_{MEASURED} \leq \mu_M + \alpha \frac{\sigma_M}{\sqrt{N}}$$  \hspace{1cm} (14)$$

In statistical literature this range is known as the confidence interval (CI). Using eqn. (14) combined with eqn. (12), we can conclude that the accuracy for arbitrary confidence is given by

$$\text{Accuracy} = V_{DUT} - \mu_M = \alpha \frac{\sigma_M}{\sqrt{N}}$$  \hspace{1cm} (15)$$

As a first order approximation, we can replace the first two terms by

$$\beta = V_{DUT} - \mu_M$$  \hspace{1cm} (16)$$

and write the accuracy equation for arbitrary confidence as

$$\text{Accuracy}_{\alpha} = \beta \pm \alpha \frac{\sigma_M}{\sqrt{N}}$$  \hspace{1cm} (17)$$

This is the fundamental equation for measurement accuracy. Since it contains the term $\sigma_M$, it is related to the repeatability (precision) of the measurement but has additional factors included. There are several ways to improve accuracy: (1) Remove the bias error $\beta$ by calibrating to a known reference value; (2) Increase the size of the sample set N to reduce the influence of measurement repeatability; (3) Decrease the intrinsic amount of noise $\sigma_M$ associated with a measurement by
purchasing more expensive instruments with a lower noise floor or by improving the DIB design and test interface.

Example:
A DC offset measurement is repeated 100 times, resulting in a series of values having an average of 257 mV and a standard deviation of 27 mV. In what range does the noiseless measured value lie for a 99.7% confidence? What is the accuracy of this measurement assuming the systematic offset is zero?

Solution:
Using eqn. (14) we can bound the noiseless measured value to lie in the range defined by:

\[
257 \text{ mV} - 3 \times \frac{27 \text{ mV}}{\sqrt{100}} \leq V_{\text{measured}} \leq 257 \text{ mV} + 3 \times \frac{27 \text{ mV}}{\sqrt{100}}
\]

or

\[
248.9 \text{ mV} = V_{\text{measured}} = 265.1 \text{ mV}
\]

The accuracy of this measurement would then be ±8.1 mV with a 99.7% confidence. Alternatively, if we repeat this experiment 1000 times, we can expect that 997 measured values will lie between 248.9 mV and 265.1 mV.

C. Test Time
Measurement accuracy is largely a function of test time. With zero systematic offset, we see from (17) that accuracy can be improved by collecting more samples thereby driving down the level of uncertainty. However, due to the square-root operation in the denominator of this expression, this benefit is limited to small increases in sample size. For instance, to reduce the uncertainty by a factor of 10, we need to collect 100 times more samples. To reduce the uncertainty by a factor of 100, we need to collect 10,000 more samples, generally an unacceptable increase in test time.

An alternative approach to deal with measurement uncertainty without suffering a time penalty is to absorb the uncertainty into the test limits. Assuming the tester has a measurement accuracy of ε, we would set the test limits according to

\[
\text{Upper Test Limit} = \text{Upper Spec. Limit} - \varepsilon
\]

\[
\text{Lower Test Limit} = \text{Lower Spec. Limit} + \varepsilon
\]

This is called guardbanding the specification limits and is illustrated in Figure 8(a). Typically, the size of the guardband (identified as the blue region) is a function of the tester accuracy and the desired CI, i.e.

\[
\varepsilon = \alpha \frac{M_{\text{CI}}}{\sqrt{N}}
\]

While guardbanding enables a faster test, it comes at a price. As is evident from Figure 8(a) and (b), the larger the measurement uncertainty, the smaller the region of acceptability; thus, leading to an increase in yield loss. Good product must be thrown away in order to minimize the risk of bad product from escaping the test.

Figure 8: (a) Guardbanding the specification limits, (b) Illustrating the implications of large guardbands on the region of acceptability.

Figure 9 illustrate the fundamental trade-offs between the defect level (i.e., escapes) and yield loss as a function of the size of the guardband. If we assume that the cost of an escape is \( C_{\text{escape}} \) and the cost of lost product is \( C_{\text{product}} \), then we can write a cost equation in terms of the number of escapes and lost product as

\[
\text{Cost} = C_{\text{escape}} \times N_{\text{escapes}} + C_{\text{lost product}} \times N_{\text{lost product}}
\]

We can superimpose this cost curve on Figure 9 and recognize that for a given amount of products, an optimum guardband exists. Semiconductor manufacturers generally consider the implications of risk much more important than cost; hence, skewing this analysis significantly towards minimum defect levels.

III. DC, AC AND DYNAMIC TESTING
Electronic circuits are used to realize algorithms in hardware using basic building blocks such as amplifiers, comparators, modulators, etc. In many
ways one can think of circuit design as the hardware equivalent to writing a computer program in software. In general, electronic circuits have a range of useful operation, limited largely by noise and distortion mechanisms. In fact, noise limits the smallest signal that a circuit can process, whereas distortion sets the upper limit of signal operation. Moreover, gain variation and offset introduces additional uncertainty in the algorithm.

Figure 9: Plot showing yield loss, defect level as a function of guardband value.

A. Signal Transmission

Signal transmission refers to the correlation between the input and output signals of a system. A straight-line behavior through the origin indicates a linear operation. Deviations from a straight-line indicate an offset or distortion mechanism, as illustrated in Figure 10. Many numerical algorithms require some form of linear operation, for example, signal-processing gain. Measuring gain and offset of a circuit is a standard test for most electronic devices.

Assuming linear behavior for a circuit, i.e.

\[ v_O = A v_{IN} + O \]  \hspace{1cm} (21)

we can solve for the model parameters \( A \) and \( O \), through two separate measurement involving \( (v_{in1}, v_{o1}) \) and \( (v_{in2}, v_{o2}) \) according to the following:

\[ A = \frac{v_{o2} - v_{o1}}{v_{in2} - v_{in1}} \]
\[ O = \frac{v_{o1} v_{in2} - v_{o2} v_{in1}}{v_{in2} - v_{in1}} \]  \hspace{1cm} (22)

Whether the attributes of the signal are DC or AC, a similar test is performed; however, there is a more efficient method to obtain the gain and offset of a circuit when AC signals are involved. This will be further discussed below in subsection III.C.

Figure 10: Transfer characteristic of an electronic circuit having a gain and offset.

B. Noise

Noise is present at the output of all electronic circuits and is caused by the random motion of thermally-excited electrons. Measurement of a noise signal is a difficult and often misunderstood topic, but one of immense practical concern. Since it is a random variable and cannot be characterized in the usual way (i.e. with an amplitude, phase or frequency), a probabilistic approach must be taken. Generally, there are two ways in which to describe noise: correlation functions in the time domain or a power spectral density (PSD) function in the frequency-domain.

The auto-correlation function is defined through an integral operation as follows

\[ R(\tau) = \frac{1}{T} \int_{-T/2}^{T/2} x(t)x(t+\tau)dt \]  \hspace{1cm} (23)

The auto-correlation function is a measure of the similarity or correlation of the noise signal \( x(t) \) with itself. The Fourier Transform of \( R(\tau) \) leads us to the Power Spectral Density \( S(f) \), defined as

\[ S(f) = F \{ R(\tau) \} \]  \hspace{1cm} (24)

where \( F \{ . \} \) signifies the Fourier Transform operation [3]. Practically, collecting the statistics associated with a noise signal in the frequency domain is more easily performed than in the time-domain with the auto-correlation function. One common test set-up involves a tunable narrowband filter and an RMS voltmeter as depicted in Figure 11. Assuming the filter with bandwidth \( \Delta f \) is tuned to a particular center frequency \( f_c \), then the power at this frequency normalized by the filter bandwidth provides an expression for the power spectral density given by
where $V_{\text{RMS}}$ is the RMS value of the signal appearing at the voltmeter input. The measurement is repeated at different frequencies leading to a PSD plot such as that shown in Figure 12. The rms value of the noise signal over any range of frequencies, say between $f_1$ and $f_2$, is simply the square-root of the area under the PSD plot, defined by

$$V_{\text{rms}, f_2-f_1} = \sqrt{\int_{f_1}^{f_2} S(f) df}$$

(26)

Likewise, the rms value of the entire noise signal is simply given by

$$V_{\text{rms, Total}} = \sqrt{\int_{0}^{\infty} S(f) df}$$

(27)

C. Distortion

Electronic circuits generally exhibit quasi-nonlinear (almost linear) behavior as shown in Figure 13. Power Series representations are often used to model their behavior, given by

$$v_O = a_0 + a_1 v_{IN} + a_2 v_{IN}^2 + a_3 v_{IN}^3 + \ldots$$

(28)

Usually terms higher than 3rd order are neglected, as they are seldom significant. Under sinusoidal input conditions, the linear and non-linear behavior of the DUT is available. Specifically, the terms of a Fourier Series description of the output signal provides information about the linear and non-linear behavior of the DUT. Figure 14 provides a simple illustration of this spectral decomposition procedure through the application of several plots of the spectral coefficients as a function of frequency. Here $S_{\text{IN}}$ and $S$ represent the input and output signal level at the test frequency $f_0$. Also, $H_2$, $H_3$, etc., represent the harmonics produced by the nonlinear behavior of the DUT. Here $H_0$ represents the DC offset and the ratio $S/S_{\text{IN}}$ is the gain of the device at $f_0$. Since the harmonics are not part of the input signal, they are assumed to be created by the DUT, and hence their magnitude provides a measure of amplifier linearity.

![Figure 11: Typical noise measurement setup.](image)

![Figure 12: A PSD plot.](image)

![Figure 13: Illustrating the nonlinear transfer characteristic of an amplifier.](image)

![Figure 14: Spectral plots of the input and output signals through a nonlinear circuit.](image)

Using sampling techniques, together with the Nyquist sampling theorem [4] (i.e., for a sinewave, we must take more than two samples per period of the highest frequency component of a signal), we are able to arrive at the spectral behavior of a circuit in the most cost effective manner.

The Fast Fourier Transform, or FFT, is a highly efficient procedure for computing the spectral coefficients. For N samples of a signal, the FFT requires $N \log_2 N$ complex additions and $(N/2) \log_2 N$ complex multiplication. This is in direct contrast to the $N^2$ operations required to solve a system of linear equations involving N spectral coefficients [4].

The FFT of a signal $x(n)$ is given by the relation

$$X(k) = X(k)e^{j2\pi kn} = \sum_{n=0}^{N-1} x(n)e^{-j2\pi kn}$$

(29)
FFT programs are available in most numerical packages such as MATLAB and Excel. In MATLAB, one would simply store the N-samples of the signal in a vector \( x \), and execute the FFT command as follows:

\[
X = \text{FFT}(x)
\]  

Here \( X \) is another N-dimensional vector containing the complex values of the frequency domain coefficients. The RMS value of the spectral coefficients, denoted by \( \bar{c}_k \) corresponding to the k-th Fourier series coefficients, is then deduced from the FFT data as follows:

\[
\bar{c}_k = \begin{cases} 
\frac{1}{N} |X(k)| & k = 0 \\
\frac{\sqrt{2}}{N} |X(k)| & k = 1, \ldots, \frac{N}{2} - 1 \\
\frac{1}{N\sqrt{2}} |X(k)| & k = \frac{N}{2}
\end{cases}
\]

where

\[
|X(k)| = \sqrt{\text{Re}(X(k))^2 + \text{Im}(X(k))^2}
\]

For frequencies above \( k=N/2 \) (the Nyquist Frequency), we make use of the symmetry in the frequency domain to arrive at the full set of spectral coefficients.

In mixed-signal test, one is often interested in various measures of goodness related to the behavior of a device, such as signal-to-distortion ratio, signal-to-noise ratio, etc. Table 1 provides a brief overview of these measures and how they relate to the spectral coefficients. The accuracy for each of these measures can be found in [5].

While the FFT of a sample signal described by eqn. (30) provides information about the total noise power \( N \) in a signal, the spectral coefficients are not in general equal to the PSD of the noise component as described in subsection III.B. Instead, an FFT of the samples of the auto-correlation function would be required to obtain a valid noise PSD.

One important discovery that has its roots in mixed-signal test is the principle of coherency [6]. In order to avoid spectral leakage effects associated with an FFT analysis, it is imperative that the signals used to excite a DUT are sub-harmonically related to the sampling frequency \( F_S \) according to the following

\[
f_T = M \left( \frac{F_S}{N} \right)
\]

This is equivalent to ensuring that the period of a test signal completes a full cycle in the time that the samples are collected over \((N/F_S)\). This is illustrated in Figure 15 for several values of \( M \).

### Table 1: Various Distortion and Noise Measures Form FFT Data.

<table>
<thead>
<tr>
<th>Distortion Metric</th>
<th>Expression</th>
<th>FFT Data (V/V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Signal to 2nd Harmonic Distortion</td>
<td>( S ) ( \frac{H_2}{C_M} ) ( C_M ) ( C_{2M} )</td>
<td></td>
</tr>
<tr>
<td>Total Harmonic Distortion</td>
<td>(\sqrt{H_1^2 + H_2^2 + H_3^2 + \ldots} ) ( C_M ) ( C_{M} ) ( C_{2M} ) ( C_{3M} ) ( \ldots )</td>
<td></td>
</tr>
<tr>
<td>Signal to Noise Ratio</td>
<td>( S ) ( \frac{N}{N} )</td>
<td></td>
</tr>
<tr>
<td>Signal to Total Harmonic Distortion plus Noise</td>
<td>(\sqrt{N^2 + H_1^2 + H_2^2 + H_3^2 + \ldots} ) ( C_M ) ( C_{M} ) ( C_{2M} ) ( C_{3M} ) ( \ldots )</td>
<td></td>
</tr>
</tbody>
</table>

### Figure 15: Coherent signals with different values of \( M \).

### IV. TEST FOR ANALOG CHANNELS AND SAMPLED-DATA CHANNELS

Analog channels are generally tested for signal impairments such as: gain and absolute level tests, frequency response tests (magnitude and phase), distortion tests, and noise and rejection type tests.

### Figure 16: Voltage-follower test setup.

To give the reader a sense of these types of tests, consider the voltage buffer test setup shown in Figure 16. A 1-V sine wave at a frequency of approximately 1 kHz is applied to the voltage buffer by the arbitrary waveform generator (AWG). The sine wave is
synthesized by the AWG using 512 samples at a rate of 10 kHz. In order to ensure coherency, 51 cycles of the sine wave were completed in the 512 points (e.g., M=51, N=512 and F_S=10 kHz). This resulted in the actual sine wave frequency being 996.094 Hz according to eqn. (33) rather than 1000 Hz. The test engineer must always contemplate the significance of this difference when performing a test. The output of the buffer is then sampled by the digitizer at 10 kHz and 512 samples are collected for FFT post-processing. The resulting spectral plot is shown in Figure 17. Here only the output signal and its harmonic distortion products are shown. The output signal resides in Bin 51 with an rms value of 1.025 V. Also, identified in this plot are the harmonic levels for H₂, H₃, H₄ and H₅. These all reside in bins that are integer multiples of the fundamental bin of 51. The signal-to-THD measure can be found from Table 1 and computed as follows:

\[
\frac{S}{THD} = \frac{1.025 V}{\sqrt{(1.23 mV)^2 + (2.54 mV)^2 + (0.78 mV)^2 + (0.32 mV)^2}}
\]

which reduces to a S/THD of 50.8 dB.

Figure 17: Example spectral plot showing only signal and distortion terms.

Sampled-data channels (such as the ADCs test setup shown in Figure 18) are tested for the same signal impairments as analog channels but quantization noise, aliasing and imaging effects associated with sampling must also be considered [7].

Figure 18: Analog-to-digital converter test setup.

V. TESTS FOR CLOCKS AND SERDES TYPE DEVICES

Many of today’s electronic devices make use of high-speed asynchronous serial links for data communications such as: USB, Firewire, PCI-Express, etc.. Such devices make use of a serializer-deserializer transmission scheme called SerDes. We shall begin by first describing the attributes of a clock signal and measures used to characterize them, as this forms the basis of a SerDes test.

A. Clocks

Computer systems, along with others, make use of a centralized clock signal to indicate the timing of the arrival of a particular bit of information as depicted in Figure 19. Here we are assuming that the flip-flops are physically separated from one another over some distance, as indicated by the transmission lines interconnecting them. Unfortunately, timing errors occur due to the physical limitation of the medium as well as noise associated with the clock. Synchronous systems are sensitive to variations in clock period, as this can cause hold-time violations leading to logic errors.

Figure 19: Synchronous clock distribution.

Noise and timing offsets or clock skews manifest themselves as errors that are phase modulated onto a desired reference clock as illustrated in Figure 20. Here \( \phi(t) \) represents the modulating error signal that includes both noise and clock skewing errors. Clock signals can be characterized by either looking at the PSD of the clock signal directly in the frequency domain using a spectrum analyzer (a method that is too slow for production testing) or by demodulating the clock signal with respect to a known reference to obtain the error signal \( \phi(t) \) directly, as illustrated in Figure 21. Once \( \phi(t) \) is found, we can obtain metrics of error signal behavior such as the mean, the rms and the peak-to-peak values. It is customary to refer to the noise aspect of this error signal as jitter. Measures like period jitter and cycle-to-cycle jitter are commonly used to describe a clock signal. These too are based on the error signal \( \phi(t) \), albeit, the first and second derivative of the error signal.

The PSD of a clock signal is shown in Figure 22 around the first harmonic of the clock; a similar behavior holds true for the other harmonics as well.
Figure 20: Timing and noise errors can be viewed as phase modulating a reference clock.

Figure 21: Demodulating a clock signal to obtain the error signal in which to quantify the performance of a clock signal.

Figure 22: Phase noise PSD plot for a clock signal.

Typically the PSD of the jitter rolls off on each side of the harmonics of the clock in a Lorentzian-kind of way. As PSD varies with frequency, data sheets often specify the worst-case PSD at a given distance from the carrier frequency $f_c$, normalized by the power of the carrier, expressed in dBc/Hz, i.e.,

$$ L(f_c) = 10 \log_{10} \left( \frac{S_{\phi}(f_c)}{P_{\text{Carrier}}} \right) \text{ dBc/Hz} \quad (34) $$

The quantity $L(f)$ is known as the phase noise.

A third strategy for evaluating noisy clocks is to make use of a statistical model of the noise behavior based on a histogram of the error signal $\phi(t)$. The idea is to assume a particular noise distribution for the jitter, e.g., the dual-dirac model consisting of two Gaussian distributions with mean values separated by the distance parameter $DJ$ (deterministic jitter) and equal standard deviation denoted by $RJ$ (random jitter). $RJ$ represents the noise in the clock signal and $DJ$ represents circuit bandwidth-related effects. While the dual-dirac method is popular, no universal approach is used to decide on the distribution parameters. This has lead to many different extraction methods; not all being equivalent. Another popular method is the tail-fit PDF fitting method of Wavecrest [8]. This approach makes no assumption of the DJ component or the symmetry of the two Gaussian distributions. Through a numerical procedure this algorithm finds the mean and standard deviation of two Gaussian PDFs based on the data in the tail region of the captured histogram, as illustrated in Figure 23. The main idea of the tail-fit algorithm is to use the data that is most likely caused by a random process and least disturbed by any deterministic or periodic signal component.

Figure 23: Illustrating the tail-fit PDF fitting algorithm.

B. SerDes Type Devices

The basic architecture of a SerDes serial link is shown in Figure 24. Beginning on the left-hand side, a set of $N$-wide bits is shifted in parallel into a shift-register called a serializer at a rate of $f_{clk}$. At the appropriate time, the bits are shifted out of this register in a serial manner at a rate of $N \times f_{clk}$. The transmitter encodes the bits into a corresponding line code, together with possible pulse shaping, for transmission over the link. The line code ensures that the phase of the local clock (transmitted side) can be recovered at the receiver end. The receiver conditions the incoming bit stream through a filtering or equalization operation and captures the data in another shift-register called the deserializer. The captured data is then shifted out in an $N$-bit parallel form at a clock rate of $f_{clk}$.

A detailed schematic of the transmitter is provided in Figure 25. A phase-locked loop (PLL) is used to translate the system clock $f_{clk}$ to higher frequency. This new clock is used to drive out the bits in the shift-register at bit rate $N \times f_{clk}$. For an alternating 01 transmitted pattern, the transmitter looks like a regular clock signal at frequency $N \times f_{clk}/2$. Measures like the mean, the rms, and the peak-to-peak jitter are used to quantify the behavior of the transmitter. Alternatively, phase noise or the PDF curve-fitting approach can be used.
For other transmitted digital patterns, the PSD will contain many spurs related to the spectrum of the digital pattern (convolution of alternating 01 pattern spectrum with the digital pattern spectrum). Jitter metrics and phase noise quantities are often too cumbersome to use here. Rather, an eye diagram such as that shown in Figure 26 is used for some pre-selected worst-case logic pattern. The eye diagram provides a time-domain view of the transmitted signal. This includes any noise effect such as jitter as well as any circuit bandwidth effects (e.g., inter-symbol interference) that limit both the magnitude of the eye opening, as well as the minimum signal amplitude transmitted. Also, the rise and fall times associated with the data transition is available. The histograms of the captured data can also be obtained from the eye diagram data; hence a PDF model of behavior can be extracted containing RJ and DJ components.

A block diagram of the receiver is shown in Figure 27; here, a clock recovery circuit consisting of a PLL and a flip-flop is shown. The PLL is used to extract the synchronizing clock signal from the incoming data stream. The recovered clock is then used to capture the incoming data stream. By design, the data should be captured at the widest opening of the eye diagram (see Figure 26).

Testing the receiver requires more care than the transmitter. The function of the receiver is to extract a data stream from the channel subject to noise, signal attenuation and bandwidth dispersion effects. Measurements on the recovered clock are necessary to evaluate the intrinsic jitter of the PLL. As this signal is a clock signal, it is evaluated using one of the methods described previously.

The input-output behavior of the receiver function is evaluated for its ability to detect the correct bit present at its input subject to a particular level of noise. The most important parameter of interest is the bit-error rate (BER) as a function of signal amplitude. One simply injects a set of known bits (usually a pseudo-random pattern) into the receiver input with a particular level of jitter induced noise and counts the number of incorrect decision levels in some predetermined time interval. The BER is then found from the equation

\[
\text{BER} = \frac{\text{Error Count}}{\text{Total Bit Count}}
\]

Most SerDes standards require a BER less than \(10^{-12}\); a very demanding level of performance and one that requires tens of minutes to perform. While this approach is sufficient for low-volume products selling
for $1000 or more, it is not suitable for high-volume runners selling for a few dollars. Instead, one makes use of the jitter extraction methods described previously, derived from the eye-diagram measurements, and extrapolate to the BER metric using a model of the receiver behavior based on the random jitter component \( \sigma_{RJ} \) and the normalized sampling instant within a bit period \( UI_{Th} \), such as

\[
BER = 0.5 \times \left[ 1 - \Phi \left( \frac{UI_{Th} - 0}{\sigma_{RJ}} \right) \right] + 0.5 \times \Phi \left( \frac{UI_{Th} - 1}{\sigma_{RJ}} \right) \tag{36}
\]

Here \( \Phi(x) \) is the cumulative distribution function for a Gaussian distribution [7]. The BER for different sampling position is shown in Figure 28. Clearly the BER is lowest when the received signal is sampled in the middle of the bit period (i.e., \( UI_{Th}=0.5 \)) and degrades quickly as the sampling instant moves towards either edge of the bit period (\( UI_{Th}=0 \) or \( UI_{Th}=1 \)).

RF devices usually process a high frequency signal \( f_0 \) over a very small bandwidth \( \Delta f \) (i.e., \( \Delta f/f_0 \) is small). In essence, RF signals are sinusoidal signals with small side bands. Circuit techniques are based on narrowbanding principles (high-Q filters) and heterodyning (frequency translation) methods. Moreover, RF circuits work with very weak signal levels in the presence of large signals, such as those transmitted in the presence of a receiver.

A different terminology is used to describe RF circuits: characteristic impedance (\( Z_0 \)), voltage-standing wave ratio (VSWR), return loss, insertion loss, s-parameters, etc. For the most part, these terms relate the incident, reflected and transmitted waves on a waveguide at the interface of two different mediums, e.g., PCB trace-to-SMB-coupler.

In a digital transmitter, such as that depicted in Figure 29, the analog/RF electronics is present in the front-end. The baseband portion of the transmitter would be implemented using digital circuits. For digital receivers, such as that shown in Figure 30, except for the front-end section highlighted by the shaded region, most of the electronics is digital.

There are many different types of RF test techniques being pursued today in research circles. They range from structured, functional, statistical-based, specification-based and correlation-based type tests. To the best of our knowledge, specification based tests continue to dominate the production test landscape. The use of correlations to simplify a test is often done today by the test engineer. However, this is generally carried out with large amounts of manufacturing data to support the particular case. Today we are seeing...
numerous attempts at capturing the essence of these correlations in faster ways and using this information to speed up the test process (e.g., alternate test [12]).

![Figure 29: Digital transmitter implementation.](image)

RF Testing can be broken up into two types of tests: transmitter and receiver tests. The transmitter is tested for the maximum power level transmitted, the linearity of the signal transmission, carrier leakage effects and flatness of the transmitter frequency response. The receiver on the other hand is tested for its sensitivity (the smallest signal that can be recovered), the maximum input level before excess distortion takes place, adjacent and non-adjacent channel rejection and I and Q phase mismatches. For the most part, these tests measure the behavior of the RF/analog circuits. Once again, the analog electronics in the transmitter and receiver are tested for signal transmission, linearity and noise. The digital circuits can be tested using standard digital test techniques such as scan and is therefore not addressed here.

A common test technique used to measure the signal quality associated with an RF circuits is to translate up a synthesized baseband signal using a mixer into the RF spectrum of the device and translate down its response using another mixer circuit. In this way, the DSP-based methods described in section III are directly applicable.

VII. IMPORTANCE OF THE TEST INTERFACE

The importance of the test interface cannot be understated. This was alluded to in the RF section; however, it is true of all test situations. Failure to consider the medium between the DUT and the tester electronics can result in large noise pick-up and signal degradation. This, in turn, can lead to a high yield-loss. In general, there is a large physical separation between the electronics in the test head and the electronics in the DUT. In fact, on the Device Interface Board (DIB), the trace length can be of the order of 1 foot (30 cm) or more. These dimensions are significant, and may extend beyond the drive capabilities of the DUT.

Consider the cross-sectional view of the test head in Figure 31. Signals propagate from the tester electronics up through the pogo pins into the DIB, through the socket and into the DUT, and back via the return path. Various discontinuities are met along the signal path, such as PCB vias, socket and pogo pins, resulting in signal loss, speed reduction, increased noise and EMI issues. Materials used to construct the PCB and the traces also have an impact on the signal integrity. For instance, the weave of the fiberglass layer in a FR4-type PCB results in a dielectric constant that is a function of board position. At very high-speeds, the roughness of the surface of a trace combined with the skin effect is fast becoming an important limitation at data rates above 20 Gb/s.

There are also environmental dependencies such as temperature and humidity (oxidation) that can affect the signal path. These generally result in measurements whose value change with time. For instance, the socket is exposed to the humidity in the local environment that causes an oxidation layer to form on the outer pins of the socket. Depending on the time of exposure and IC insertion pressure, a small but time-varying resistance appears in series with the DUT. This resistance can create havoc on small value resistance measurements.

VIII. DESIGN FOR TESTABILITY

The electronics in the test head of an ATE generally lags behind the performance capability of the DUT. Generally, this manifests itself into a situation where the DUT channel capacity exceeds that of the ATE. Here channel capacity, C, is based on Shannon’s definition [13], i.e.,

$$C = \frac{S}{N} \times BW$$

where S is the rms value of the signal, N is the rms value of the noise and BW is the bandwidth of the channel.

As an analogy, we model the channel associated with the DUT in Figure 32 as a wide pipe (large bandwidth, large SNR) connecting to a narrow pipe associated...
with the ATE instrument. Clearly, at the interface of these two pipes, a discontinuity exists; not all the information can get through, something has to be lost. In practice, the test engineer has to run a test at reduced speed or compromise the resolution of the information collected. This is clearly an undesirable situation.

In this section we will consider the options a test engineer has to circumvent the performance limitations of the tester. In a general way, we refer to these improvements as Design-For-Test (DFT) methods or techniques, as the test engineer must find a system-level solution that trades off many factors, such as business concerns with numerous technical issues.

A. DIB Electronics

In order to improve the measurement capacity of the ATE, the test engineer can add electronics to the DIB as shown in Figure 33. This enables the measurement electronics to be placed closer to the DUT, improve the signal integrity, as well as enable the test engineer the use of state-of-the-art components to construct new instrumentation. We often see buffers, instrumentation amplifiers, mixers and other types of signal conditioning circuits added to the DIB. Today, FPGAs are fast becoming popular DIB components, as well as 24-bit high-resolutions ADCs.

An important problem associated with the DIB approach is the fact that the test engineer often overlooks the need of a robust solution, one that is insensitive to temperature effects as well as one that is insensitive to variations in component values. The lack of circuit robustness often comes back into the picture once the DIB solution is introduced into the manufacturing environment, where issues of correlations between different DIBs, correlations across different factory installations, and other issues, are important concerns.

B. Loop-Back Approach

Another approach that is often used by the test engineer is the loop-back approach. This applies to those ICs that have both a transmit and receive function on a single die. The loop-back approach has the advantage that only a relay is needed to create a by-pass function. No other electronics components are needed, as the DUT internal electronics will be used to perform the measurement function (more like a decision, though). One such example is illustrated in Figure 34 for an arbitrary transceiver-type device. Here the loopback is placed on the analog side of the device but could just as easily be placed on the digital side.

The analog side is often chosen, as it is on this side where the measurement difficulties arise.

The loop-back approach was first introduced with the voice-band CODECS in the early 80’s [14]. These were the very first mass produced mixed-signal ICs; however, during this time, some very significant measurement issues arose. The most significant issue
was that of fault masking and this lead to excessive levels of device escapes. Process related changes in component behavior can cause different behaviors in the transmit and received sections of the ICs. Moreover, these changes can cancel out making a bad device look good. Today, the loop-back approach is used to identify gross failures quickly. It is generally not used as a single channel test, rather it is used in combination with other tests.

One final remark about the loop-back approach is its lack of traceability. No measurement is being made with respect to a known reference, hence there is no way to identify weakness in the manufacturing process to enhance yield; in other words, nothing is being learned.

C. Golden Device Approach

The golden device approach aims at eliminating the fault masking effects of the loop-back method. This approach aims at splitting the transmit and receive functions between the DUT and another DUT-like device on the load board. The goal is to perform separate transmit and receive channel tests. Here two identical devices are used in this approach. Referring to Figure 35, the method is as follows: first the DUT is placed into test mode and data is moved into the DUT for transmission back to the ATE. Data is prepared in the ATE for transmission to the DUT through the golden device. Data is exchanged between golden device and DUT. The DUT received data is sent back to ATE for decision. Channel decisions are made by separately comparing the transmit and receive data from both channels (DUT and golden device). The DUT is then removed from the socket and replaced with a new DUT while the golden device remains on the DIB.

The main drawback of this approach is that it is a Go/No-Go test, measurements are not traceable back to any reference standard. Also, results will drift with temperature. In addition, as the specifications of the DUT and golden device are similar, the measurement noise will be doubled (in a power sense) resulting in greater yield loss.

D. Built-in Self-Test

An embedded test approach that falls in the DFT realm involves placing focused test instruments directly inside the DUT. This is commonly referred to as Built-In Self-Test or BIST. Adding embedded test circuits directly on-chip made of silicon material has been an important design goal for mixed-signal test researchers for several decades now. Today, most high-speed circuit designers are constructing some form of BIST to aid the characterization of their device, e.g., [15].

State-of-the-art measurement instruments use materials other than silicon (GaAs, InP) for their front-end electronics and, generally, have better performance than silicon. However, the performance gap between silicon and group III-V materials is being compromised by the interconnect performance loss associated with the ATE interface. It is becoming clear to many that the performance advantage of a group III-V material will have a performance advantage only if the interconnect is kept short and uniform, something that is hard to do on a tester with PCB vias, sockets, time-varying contact resistance and other discontinuities.

Over the past decade, many different circuit functions have been created from spectrum analyzers, oscilloscopes, voltmeters, waveform generators, probes, etc. [16]. For the most part, these circuits consume very little silicon area. This leads us to believe that the research thrust is not so much on the creation of new IP, but rather on how to make the circuits more robust to process variations, power supply and temperature effects. At this stage of BIST development, little if anything has been done to address this issue. It is the authors’ belief that a design-for-test-with-feedback method needs to be developed that encompasses the robustness requirements of a
production test environment. Moreover, the question of how an embedded instrument can make an accurate and repeatable measurement when it has performance very similar to the device-under-test needs to be answered.

IX. CONCLUSION

In conclusion, a brief overview of mixed-signal test for production was described. The discussed topics included some material on analog, mixed-signal, SERDES, and RF testing. Also, it was reported that test engineers invoke some form of DFT to solve ATE related test problems. The approaches described include load-board design, loop-back and golden device testing, and embedded instrumentation or BIST. All in all, this paper has shown that mixed-signal test engineering is multi-faceted endeavor with many problems still facing the engineer.

REFERENCES