

# Afternoon Panel Discussion\*

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1:00 pm

## Hidden Quality, Crouching Customer - How Much Does the Quality of EDA Tools Impact Electronic Design?



*Moderator*

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### Description

In today's fast-paced electronics market, design engineers face incredible challenges keeping up with increasingly complex technology and time-to-market pressures. Many design engineers facing these challenges say that quality problems with their EDA tools cost them dearly in lost productivity and in missed deadlines. At the same time, the same design engineers also say that they urgently need better technology, features, and special functions in the EDA tools they use in their work.

Thus, Quality in EDA products is crucial to customer success - or is it? How much quality is enough to keep the industry moving at its fast pace? Is quality a hidden dragon that could cause customers to crouch in fear? What are the costs and who will pay for higher quality? Can EDA customers have their cake and eat it too?

Examples of some provocative questions that can be posed are:

"For the user - is EDA quality worth the hype at the expense of technology?" "Do mainstream and power users want higher quality or more functionality?"

"Do users of front-end and back-end tools require different level of quality?"

This panel will examine the core issues of quality in EDA products and the impact on electronic design — from the viewpoints of customers, EDA vendors and independent analysts.

### Panelists

Rahul Goyal, Director, EDA Business and Technology Programs, Intel Corporation

Rich Goldman, Vice President, SVP, Quality and Interoperability, Synopsys, Inc.

Rob Mains, Senior Design Automation Architect, Sun Microsystems

Scott Sandler, President and CEO, Novas Software

Gary Smith, EDA Director and Chief Analyst; Dataquest

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## Panelists Statements



**Rahul Goyal**, Director, EDA Business and Technology Programs, Intel Corporation

In spite of significant efforts by EDA companies to deliver high quality/robust tools, their customers assume the s/w will have “bugs”. While the focus is on “show-stoppers and high” impact bugs, even medium and low impact bugs can be problematic to a project approaching tape-out. The other perennial debate is whether it’s a bug or an enhancement.

So the de facto “quality cycle” in EDA is a reactive model. Customers assume there will be bugs (or missing features), and expect the suppliers to fix them. The primary variable is turn-around time. Therefore, the customer’s primary concern is the supplier’s responsiveness.



**Rich Goldman**, Vice President, Strategic Market Development, Synopsys, Inc.

EDA vendors are constantly striving to balance competing challenges — customers requesting development of new technology of increasing complexity in shorter and shorter time lines, and, at the same time, demanding “zero defects” in the shipped products and prompt response to quality issues during their chip design cycle. EDA vendors have the same tight resource constraints as their customers in this tight economic climate. Often, when balancing time-to-market pressures, product team resources allocated to new technology development come at the expense of resources for a higher level of quality.

Depending on specific EDA tool needs, EDA development engineers today allocate 40%-80% of their time to Quality: Both pro-active efforts to develop and test higher quality software and Re-active efforts to fix bugs reported by the customer. Are these the right balances from customers’ viewpoint? How much quality is enough to keep the industry moving? Who should pay the cost of higher quality level? These are typical questions that EDA customers and EDA suppliers are struggling with.

As we continue this struggle, Synopsys believes that Quality is the fundamental cornerstone of any EDA organization – not an expendable luxury. We continue to deploy advanced quality processes that utilize “best-in-class” software engineering techniques for proactively improving our software development and testing practices. This way, we can deliver on our customers’ request for new technology of increasing complexity in shorter time lines, and, at the same time, we continue to improve the quality of our software



**Rob Mains**, Senior Design Automation Architect, Sun Microsystems

Good grammar or good taste: what microprocessor developers really want from EDA Tools? The microprocessor design and development environment presents unique challenges for the design engineer, the application engineer, and the design automation developer.

The microprocessor designer is a very demanding customer, extolling the need for solutions to the complexity of the design problem, yet wanting absolute tool stability many months prior to tapeout such as not to slip schedule based on tool bugs. Examples of difficult design and analysis problems abound, both in analysis and construction tools, which exist in the presence of ever more challenging design constraints and performance goals.

These issues demand innovative design and analysis techniques, which transcribe into new algorithms and tools. How does one assure that the new functionality is of sufficient quality to provide correct results to the design team? Can adequate test and regression structures be put in place to provide a minimal guarantee of quality of results?

The above challenges are difficult to manage for both the microprocessor design team and the design automation supplier. New tools and algorithms require extensive testing not only by the design automation tool supplier, but also by the CAD team and the design team. As a result, stability has tended to be favored over increased functionality, but at a price: design performance and guarantee of tapeout quality.



**Scott Sandler, President and CEO, Novas Software**

In a sense, EDA customers want their cake and to eat it too. Advanced technology is the crouching tiger that they expect to get them to market ahead of their peers who do not adopt it as rapidly. But quality issues are the hidden dragon that can consume those gains.

Quality includes correctness of results, intuitiveness of human interfaces, completeness of interoperability and performance. Customers have a right to expect vendors to make a concerted effort toward high achievement in all these areas, and to respond immediately when tool quality compromises design schedules. They also have an obligation to participate in the quality process.

Only when customers provide high-quality input on their real needs and will vendors make the right tradeoffs. And customers cannot expect vendors to create the test cases required to adequately confirm tool functionality. Only end users have designs sophisticated enough to stress the corners of the tools. They must either share these with vendors, or continue to expect testing to continue at their sites when they receive the latest versions of tools.



**Gary Smith, EDA Director and Chief Analyst; Dataquest**

EDA tool Quality, primarily revealed by interoperability, stability, ease-of-use, performance, and quality of results is the friction in the design process. In the ITRS 2001 roadmap we took the first steps in trying to measure the cost of interoperability. The results were staggering. At best these issues add 50% more to the cost of a tool, and sometimes get close to doubling the cost of that tool. In addition to the cost of interoperability, other quality issues may cause customers additional person-months of effort and schedule delays. Millions of dollars are at stake for each and every design group. This is an issue that has been ignored for far too long.