

Benchmarking Technology for Configurable Computing System

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Abstract

A configurable computing system refers to a system that can be changed in basic computational structure, either statically or dynamically, without adding physical hardware devices. In its current realizations, such a system consists of a set of general-purpose processors augmented with a set of coprocessors, such as uncommitted Field-Programmable Gate Arrays (FPGAs). An overview of current configurable computing technology can be found in a recent article [1].

Although much attention has been given to the development of new, innovative architectures for configurable computing and investigating potential applications of this technology, little effort has been invested in developing assessment techniques for configurable computing systems. These techniques can be used to determine which systems will best satisfy a user's overall requirements, and how configurable tools and architectures can be improved. Benchmarking is commonly used for evaluating the hardware and software of general-purpose computer systems and parallel machines. As configurable computing technology matures and as new configurable architectures emerge, the use of appropriate benchmarking technology will play an increasingly important role in evaluating configurable systems. The need for objective configurable computing benchmarks has been expressed recently by several researchers [2].

This paper presents benchmarking technology for assessing configurable computing systems. An important goal of this technology is to provide benchmarks that expose as much information as possible about a configurable computing system's infrastructure, both tools and architecture. The intent of these benchmarks is not solely to compare competing architectures, but rather to provide insight regarding specific properties of configurable computing systems. The benchmarking technology leverages the work performed in the C³I Parallel Benchmark Suite (C3IPBS) program [3], which

addressed the development of a suite of benchmarks for a variety of critical C³I applications on various parallel machines. Several benchmarking concepts from the C3IPBS program have been applied to the domain of configurable computing, such as the development of a benchmarking methodology, benchmarking procedures, unbiased specifications, and acceptance tests for ensuring that an implementation satisfies a benchmark specification.

The benchmarking technology presented in this paper differs from earlier works, such as those based on *functional benchmarks* that measure end-to-end execution time, in several respects. Our approach introduces the concept of *stressmarks*, benchmarks that focus on a specific characteristic or property of the configurable computing system's infrastructure. It requires identifying a specific property of interest to be assessed, developing a stressmark that adequately measures this property, and deriving associated metrics of interest. This approach is fundamentally different from existing benchmarking approaches for configurable computing. It arises as a natural consequence of the numerous degrees of freedom and trade-off opportunities offered by configurable computing technology.

Our benchmarking approach addresses a broader class of configurable architectures and issues than existing approaches. We are looking at configurable architectures that consist of single configurable devices, multiple configurable devices, and mixed architectures, such as fixed-plus-variable devices and hybrid systems. In addition, we are addressing issues such as run-time reconfiguration, an important aspect of configurable computing architectures.

As mentioned earlier, our approach leverages existing benchmarking technology for parallel computers. It adds rigor to the benchmarking process through the development of a benchmarking methodology, and benchmark specifications for each of the benchmarks.

The approach to developing the technology includes performing the following tasks:

- Requirements Summary - review a broad range of applications and metrics to identify benchmarks that are relevant to configurable computing;
- Methodology Development - develop a rigorous methodology for benchmarking the performance, ease of design, and architectural flexibility of configurable computing systems;
- Benchmark Development – develop unbiased benchmark specifications for five stressmarks that focus on what is to be implemented, not how;
- Benchmark Evaluation - implement each stressmark on at least one target configurable computing system;
- Public Dissemination - address the public availability of the benchmarks.

In this effort, the following characteristics of a configurable computing have been selected: versatility, capacity, timing sensitivity, scalability, and interfacing. These characteristics define the stressmarks.

- 1) **Versatility** - A benchmark consisting of a distinct, sequence of operations (steps), which need to be performed on a configurable device. This benchmark stresses the infrastructure's ability to perform a variety of operations, using appropriate space-time trade-offs, in a prescribed order as efficiently as possible. For example, dynamic reconfiguration at each step may be required.
- 2) **Capacity** - A benchmark that evaluates the usable capacity of a configurable device. This benchmark stresses the infrastructure's ability to implement a large amount of logic.
- 3) **Timing Sensitivity** - A benchmark that evaluates the infrastructure's ability to effectively implement timing critical computations. This benchmark stresses various aspects of CAD tools, such as their ability to place and route effectively, in addition to the architecture.
- 4) **Scalability** - A benchmark that needs to be distributed onto a multi-device, configurable computing system. This benchmark will evaluate how effectively a design can be partitioned, along with the overall benefit achieved due to the use of multiple configurable devices.
- 5) **Interfacing** - A fixed-plus-variable or hybrid system benchmark where the "variable" part must interface to a fixed, general-purpose or digital signal processor. This benchmark stresses the interface between the fixed component (software running on the processor) and the variable component (configurable device), along with any interfaces required for input/output. This benchmark can be potentially used to evaluate hardware/software co-design [4] approaches as well.

Each stressmark defines two classes of metrics. Primary metrics reflect the property being stressed by the benchmark. Secondary metrics provide supplemental information, though implementers will only maximize the primary metrics of the stressmark. Additionally, metrics that apply to all stressmarks, for example, power, area, and cost, will also be reported.

At this time, we have developed specifications for the versatility, capacity, timing sensitivity, and interfacing stressmarks. These stressmarks are based on kernels performing image compression, Huffman encoding, CORDIC vector rotations, and morphology, respectively. We have also implemented the low complexity version of the versatility stressmark, the capacity stressmark, and the timing sensitivity stressmark on an Annapolis Micro Systems WILDFORCE board. This board contains a supervisor Xilinx 4025 FPGA and four Xilinx 4013 FPGAs. Each 4013 has access to 2 Mbytes of local SRAM.

Specifications and implementations for the remaining stressmarks will be completed by May of 1998. At that time, a benchmarking methodology document, the stressmark specifications, sample "C" and VHDL files for each specification, and implementation results will be made available on a publicly accessible WEB site. For more information, please see our WEB site: <http://www.htc.honeywell.com/projects/acsbench>.

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