Testing Embedded Memories: Is BIST the Ultimate Solution?

An ASIC Designer's Point of View

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1 Introduction

System on chip design using cores has become an integral part of todays chip design methodology. However, designers face many challenges in core testing. Random access memories are the densest circuits fabricated today. Because their transistors and lines are packed so closely together, embedded RAMs suffer from very high average number of physical defects per unit of area compared with other core types. As direct controllability and observability of embedded memory cores are low, built-in self-test techniques are widely used in embedded memory testing.

2 Realistic Fault Models

Embedded memories like ROMs, SRAMs or DRAMs have a highly regular layout. Thus researchers have investigated into techniques as inductive fault analysis or layout dependent fault analysis in order to find the impact of physical defects to electrical faults. In addition the faults may be weighted according to the probability of their appearance. With this technique realistic fault models have been found for different memory types.

Stuck-at faults, transition faults, coupling faults, and pattern sensitive faults are widely recognized classes of faults occurring in random access memories. Pattern sensitive faults arise primarily from high densities and the related effect of leakage currents in capacitive coupling between cells that are physically adjacent. As RAM densities increase, pattern sensitive faults probably become the predominant faults.

3 Built-In Self-Test

Most built-in test methods for VLSI are based on pseudorandom patterns generated within the circuit itself. While these patterns are usually effective for testing combinational logic, they are not very efficient at testing random access memory. With random test stimuli, an average of 48.5 accesses per address would be needed to ensure with a 99.9% confidence that all cells for stuck-at faults have been tested. For large RAMs with many addresses, this long test is impractical and moreover too inaccurate. To shorten the test sequence, and especially to cover more realistic RAM specific faults, many techniques exploit the regular structure of a RAM, using deterministic algorithms to create test sequences. In contrast to that pseudorandom memory tests do not require knowledge of the physical topology of the memory cell array, however they have the disadvantage that their fault coverage is probabilistic.

4 ASIC Designer's Need

BIST structures represent efficient solutions in the design for testability methodology. BIST methods for embedded memories have to consider a number of user requirements. The test algorithm has to be based on a realistic fault models, cover a very large percentage of faults and has to be cheap. Depending on the application domain of the ASIC, different goals have to be fulfilled. In order to design an ASIC for a consumer products, low cost and short time-to-market may be primary goals. In this case BIST may keep the testing time for external testers low and thus may certainly be the best way to test embedded memories.

On the other side there are applications which cannot afford failures and probabilistic fault coverage rates. Imagine an ASIC in an automotive application like an air-bag controller. If just one air-bag of a car driving on a highway will be activated unintentionally, the car company gets a serious image problem. This means that the fault coverage of the test set has to be extremely high. If just one out of one million tested chips is wrongly judged as fault free (fault coverage 99.9999%), the goals of the car company are certainly not fulfilled.

The fault coverage rate of the BIST for embedded RAMs needs special attention. If the trade-off between area and test quality moves towards quality, different BIST methods adapted for different memory types are necessary to guarantee the necessary quality. Thus the answer to the question, who should design the BIST controller, is definitely not the ASIC but the memory core designer. The ASIC designers need are BIST compilers for ROMs, SRAMs and DRAMs which are able to quantify the fault coverage rates based on realistic fault models. BIST black boxes are not acceptable for high quality demands.

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