

**Plenary Address:**  
**Building Yield into Systems-on Chips for Nanometer Technologies**

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Philippe Magarshack graduated from Ecole Polytechnique and Ecole Nationale Supérieure des Telecommunications in Paris, France in 1985. He participated to the design of the 32-bit microprocessor family of AT&T Bell Labs from 1985 to 1989, in New Jersey, Pennsylvania and California. In 1989 he joined Thomson-CSF in Grenoble, France, and took responsibility for libraries and ASIC design kits for the military market. In 1994, he joined SGS-Thomson's (now STMicroelectronics) Central R&D Group, where he now heads the central CAD and library activities, providing design solutions for ST's Systems-on-Chips in CMOS and BICMOS processes in 0.25 $\mu$ m, 0.18 $\mu$ m, 0.12 $\mu$ m and 90nm technologies, serving applications in consumer, wireless, wireline, computer peripherals, automotive and smartcards.