

SoCs with MEMS ?

Can we include MEMS in the SoCs design and test flow ?

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Abstract

Recent developments in the field of MEMS indicate a clear move toward systems, rather than just individual components. Design and fabrication of these components include new methods and techniques. Does testing require new methodologies and tools ? Will we be able to include MEMS in the SoCs flow ?

Position Statement S. Mir : MEMS are analog components. Embedding them in highly integrated devices means new test challenges for the analog and mixed-signal test community due to the multiple energy domains considered. Failure mechanisms and reliability are poorly understood and structured test approaches are generally missing. Functional testing of MEMS parts may be unavoidable, together with the use of expensive test equipment able to deal with signals other than electrical. Extremely high test costs together with poor reliability of MEMS blocks are major obstacles to see this type of cores in the SoCs of the near future.

Position Statement H. Kerkhoff : Firstly, in contrast to conventional microelectronics and current SoC, many MEM device specifications are quite dependent on the final packaging implementation, as this determines the interaction between the actual domain and the electronic voltage or current and vice versa. Hence, models of MEMS in which the influence of packaging is not or partially included will therefore not be sufficiently accurate to be used in practice. This will involve much additional research, and data to be given by core providers. As a result, designers will probably be forced to use predetermined (and modeled) packages for these devices, which will be a new issue in SoC design and test. Secondly, in many cases, for several parts of MEMS (e.g. mechanical valves) it will not be feasible to develop a direct test in a mass-production environment, unless full functional tests are allowed. In this case, special Design-for-Test structures should be included in the MEMS to transform non-electrical properties into electrical ones, e.g. via capacitances (movement to electrical property). These should be part of the data given by core providers as well as standards for MEM tests.

Position Statement S. Blanton : Are new testing methodologies and tools needed for SoCs with MEMS? The answer is unquestionably "yes". MEMS, in the most general sense, are sophisticated, miniature transducers that convert one type of energy (mechanical, thermal, optical, etc.) to another type (typically electrical) or vice-versa. Maximally testing MEMS in an all electrical domain would allow existing tester hardware to be utilized. Unfortunately, this is not possible given the mixed-physics properties of MEMS. For example, accelerometers must be literally "shaken" to provide the mechanical input stimulus needed to test and calibrate the interface between the mechanical and electrical components. Similarly, the test of other MEMS will require non-electrical stimulus generators and output response analyzers in order to test and assess their behavior. In addition, any attempts to implement MEMS structural test will require an understanding of the defect types and consequent misbehaviors. It is unlikely that this understanding will stem from an extrapolation of the defect types found in purely electronic systems. Moreover, the defect types will most likely depend on the type of MEMS and its underlying technology. For instance, defects for accelerometers and gyroscopes will be quite different from those affecting fluidic-based MEMS. Similar to analog and mixed-signal test, it is not at all clear if a structural approach to MEMS test can be successful. Therefore, new research is needed to understand the failure modes of MEMS in order to effectively develop testing methodologies for SoCs that contain MEMS.

Position Statement H. Bederr : The number of transistors integrated in a single chip has constantly increased in the past years following more or less what has been predicted by Moore's law. Systems On Chips were among the first to take advantage of this by increasing both their size and complexity. However, the use of mixed signal or MEMS blocks in Systems On Chips has not followed this trend. The major reasons for that are the technical challenges of mixing and testing two different technologies. Although some DFT techniques like PLL or ADC BIST have started to emerge, almost nothing has been proposed for MEMS testing. Designers are already looking at having MEMS blocks in RF chips used in wireless applications, for instance micro-switches, micro-electromechanical filters and antennas. What will be the impact of testing these parts on both the ATE and digital blocks ? Inserting test wrappers for both accessing and isolating these parts could follow some rules already defined for testing SoCs (like the ones resulting from the P1500 group activities) but what about the other issues : translating electrical characteristics into mechanical or optical ones, usable in a go/no-go BIST approach, automate the test insertion, adapting the ATE equipment to fit VLCT conditions ...